7970B/E Maintenance Seminar Outline

Mon: Brief Introduction
Arrange Manuals
Correct Manuals 07970-90886
07970-90887
Overview (history)
Lab: 7970B or E Alignment per handout

Tue: Magnetic tape characteristics
NRZI/PE differences
Tape path characteristics
NRZI/PE tape formats
Lab: 7970B or E Alignment per handout

Wed: Power Supply - Power Distribution PCA
Power Regulator PCA
Lab: practical application

Reel Servo PCA - Reel Servo PCA + Control & Status PCA
Lab: practical application

Capstan Servo PCA - Cap Servo PCA + Cntl & Status PCA
Lab: practical application

NRZI Write Elect - Head Assy
Resistor Load PCA
Write Control PCA
Write PCA
Control & Status PCA

Thu: NRZI Read Elect - Read Head Assy
Preamp PCA
Read Control PCA
Read PCA
Lab: practical application

PE Tape Format
PE Write Elect - Write Control PCA
Write PCA
Resistor Load PCA
Control & Status PCA
Lab: practical application

PE Read Elect - Preamp PCA
Decode PCA (Master & Slave)
Fri: Data & Status PCA
Read Control PCA
Lab: practical application

NRZI Interfaces - 13181 (Brief overview)
13183 (Brief overview)
13184 (Brief overview)
HP-IB Interface - (Brief overview)
Lo-Boy Cabinet - (Brief overview)

HP 7970B/E MAGNETIC TAPE DRIVES

I. Introduction
   - A. Objectives
   - B. Overview
     1. Overall Block Diagram
     2. Examine Course Outline and Content

II. Magnetic Tape
   - A. Why Magnetic Tape
     1. Large Storage Capacity
     2. Low Cost
     3. Reusable
     4. Medium Record/Reproduce Speed
     5. Stability (temperature)
     6. Only Interchangeable Media
   - B. Disadvantage
     1. Serial Access Only
     2. Slow Access Compared To Discs
   - C. Environmental Limitations
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     2. Deterioration
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        b. Humidity
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     2. Self-contamination
     3. Wrapping Tension
     4. Edge Damage
     5. Poor Environment
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     2. Proper Winding On Reel
     3. Handling Of Reel
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     2. Cupping
     3. Thickness
     4. Cut Skew
   - G. Tracks
     1. ANSI Versus IBM
     2. Most Significant Bits Toward Center Of Tape
   - H. Life
     1. Errors Versus Full-Reel Passes
     2. Loose Oxide - Early Life Errors

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     1. Logic "1" For Flux Transition
     2. Logic "0" For Constant Flux

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   2. Format
   3. Records
C. Parity
   1. Lateral
      a. Nine Track Odd Parity
   2. CRCC
      a. Insered By Controller
      b. Resembling Diagonal Parity
      c. Occurs Four Byte Times Following Last Data Byte
   3. Longitudinal
      a. Even Parity Within Channel
      b. Occurs Four Byte Times Following CRCC
   4. Error Correction Philosophy
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   3. One-half Inch or Larger Interrecord Gap
   4. Tape Mark Is 23_8, Recognized By The Controller
   5. Density
E. Start/Stop Time
   1. Interrecord Gap $\geq$0.5 Inches (ANSI Spec)
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   2. Construction Of Pole Pieces
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B. Simplified Tape Movement Electronics Block Diagram
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- D. PE Versus NRZI Format
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     a. Write Reset Does Not Exist For PE
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- B. Read Electronics
  1. Skew Buffer Operation
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  6. Inputs/Outputs Of Read Control PCA
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X. Troubleshooting Aids
- A. PE Test Tape

XI. Interfaces
- A. 13181A Block Diagram
  1. PCA1 Circuits
  2. PCA2 Circuits
- B. 13183A Block Diagrams
  1. PCA1 Circuits
  2. PCA2 Circuits
- C. HP-IB

I. INTRODUCTION

A. Objectives

1. This course is intended to be at level four-hundred (400).
2. Individuals completing this course will be trained to the Technical Support Engineer (TSE) level, and will be capable of training customer engineers (CE's) to the two-hundred (200) level.

B. Overview

1. General overall block diagram
   a. Indicate on the block diagram the functional groupings such as transport electronics, read electronics, write electronics, etc.
   b. Discuss I/O and signal flow.

2. Examine course outline and content

II. MAGNETIC TAPE

A. Reasons for favoring magnetic tape

1. Large storage capacity
2. Low cost
3. Reusable
4. Medium record/reproduce speed
5. Stability (temp.)
6. Only interchangeable media

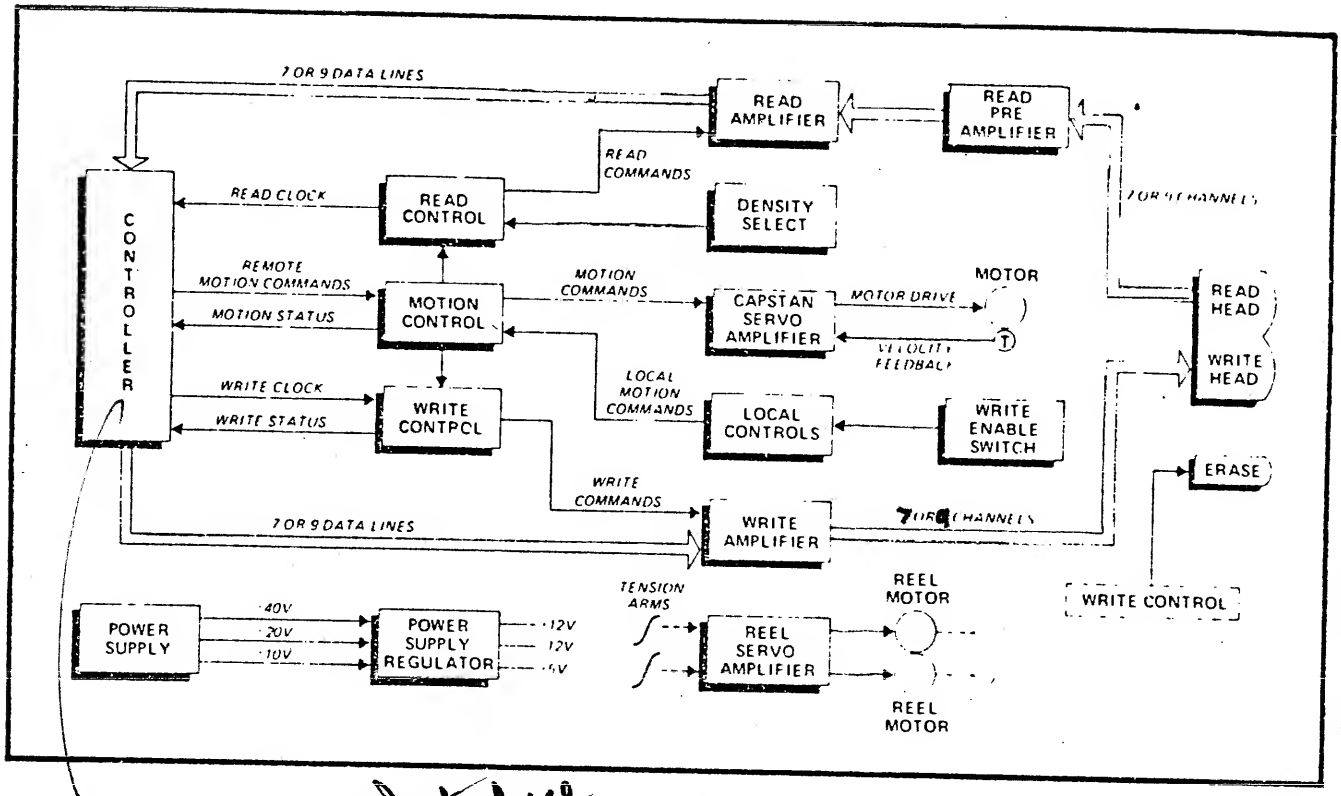
B. Disadvantages

1. Slow access time compared to disc
2. Serial access

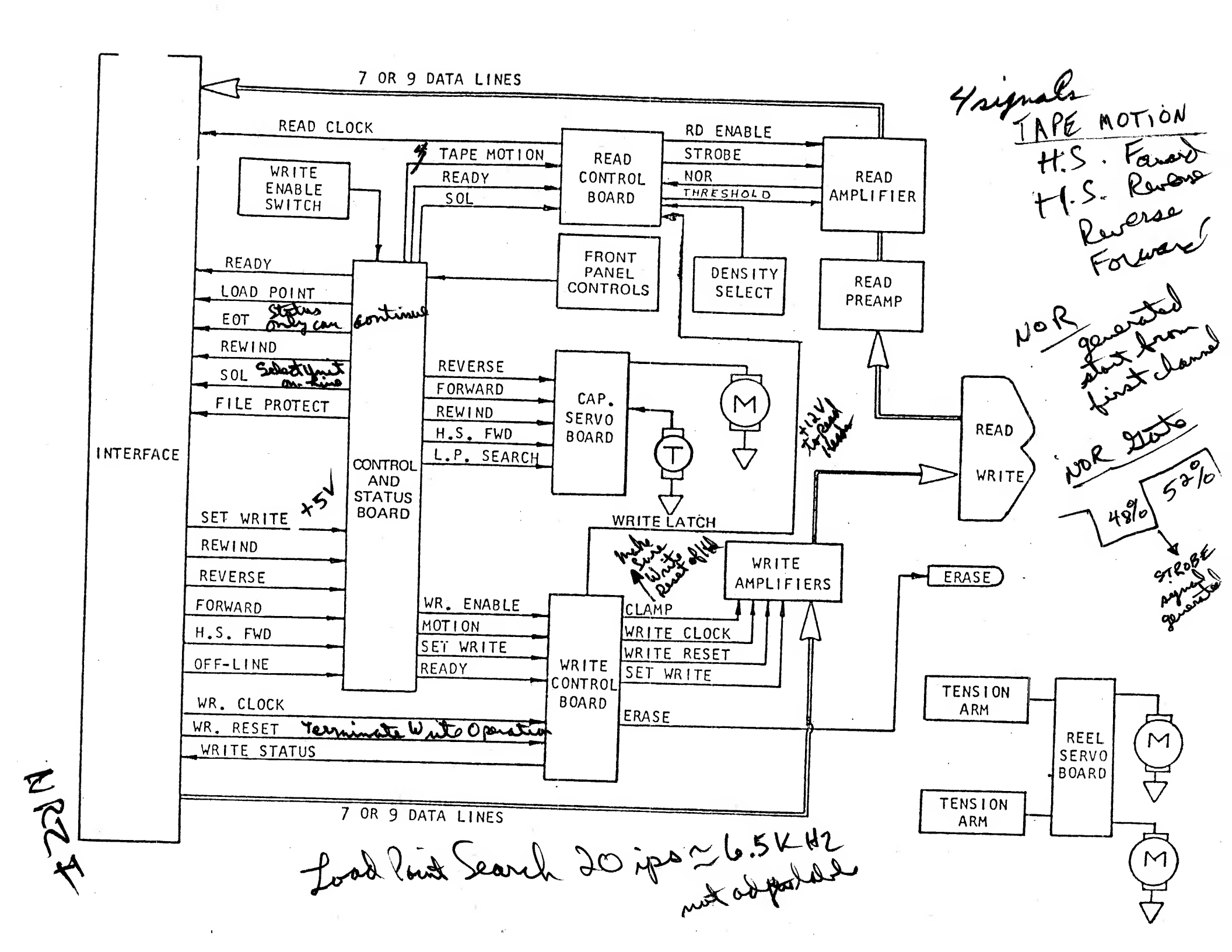
C. Environmental limitations

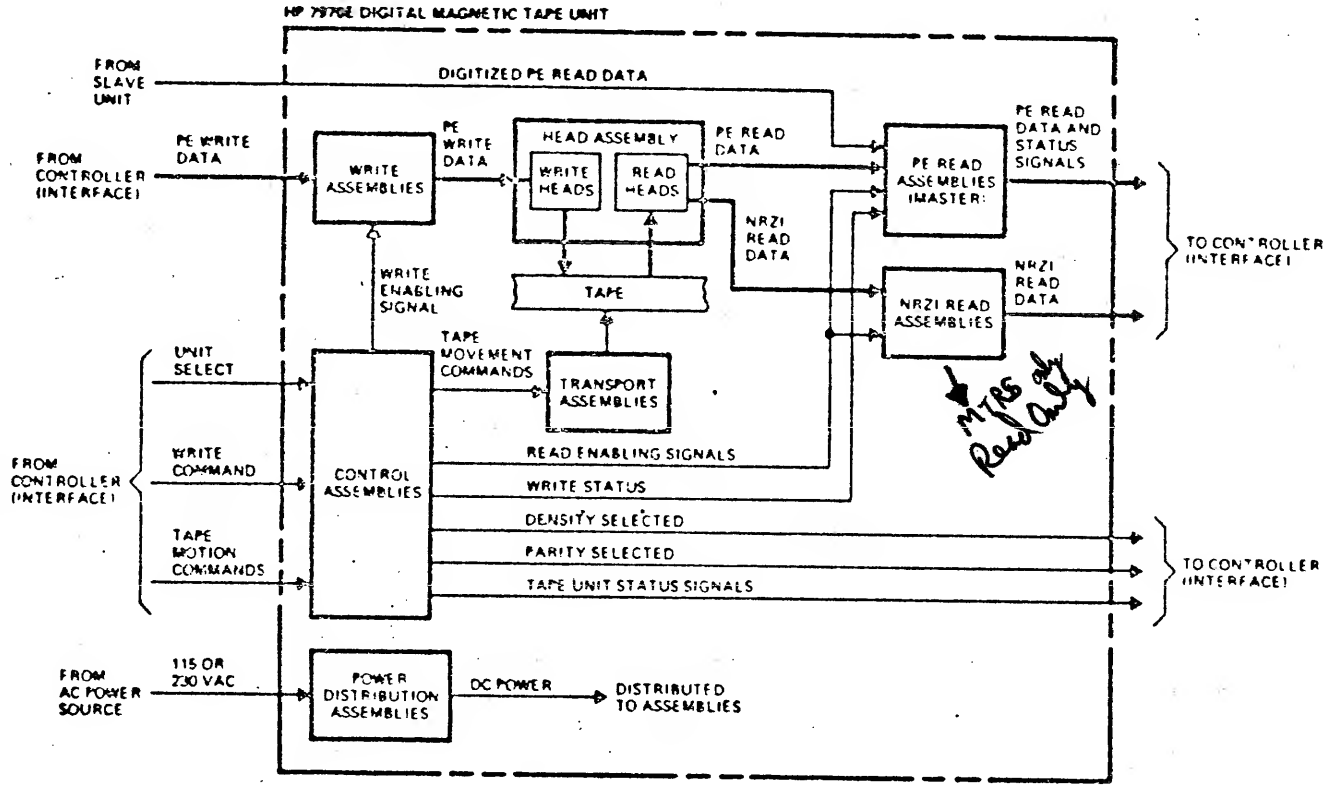
1. Dirt, lint and dust
   a. Causes dropouts
   b. Reduction in signal output
   c. Food, drink and smoking should be prohibited in tape areas (smoking due to ashes).

BLOCK DIAGRAM OF ELEMENTS



Computer Interface


7 OR 9 DATA LINES
READ CLOCK
TAPE MOTION
READY
SOL
WRITE ENABLE SWITCH
READ CONTROL BOARD
RD ENABLE
STROBE
NOR
THRESHOLD
READ AMPLIFIER
FRONT PANEL CONTROLS
DENSITY SELECT
READ PREAMP
READY
LOAD POINT
EOT
REWIND
SOL
FILE PROTECT
INTERFACE
CONTROL AND STATUS BOARD
REVERSE
FORWARD
REWIND
H.S. FWD
L.P. SEARCH
CAP. SERVO BOARD
M
T
+12V
READ
WRITE
SET WRITE
+5V
REWIND
REVERSE
FORWARD
H.S. FWD
OFF-LINE
WRITE LATCH
WRITE AMPLIFIERS
ERASE
WR. ENABLE
MOTION
SET WRITE
READY
CLAMP
WRITE CLOCK
WRITE RESET
SET WRITE
WRITE CONTROL BOARD
ERASE
WR. CLOCK
WR. RESET
WRITE STATUS
TENSION ARM
TENSION ARM
REEL SERVO BOARD
M
M
7 OR 9 DATA LINES
NRZI
4 signals
TAPE MOTION
H.S. Forward
H.S. Reverse
Reverse
Forward
NOR
generated
start from
first clock
NOR Data
52%
48%
STROBE
signal
generated
Load Point Search 20 ips ≈ 6.5 KHz
not adjustable



NOTE 1. A MASTER UNIT IS SHOWN. HOWEVER A SLAVE UNIT IS THE SAME EXCEPT THE ONLY OUTPUT OF THE SLAVE UNIT PE READ ASSEMBLIES IS PE READ DATA SUPPLIED TO THE MASTER UNIT.

Composite Tape Unit Block Diagram

WHY MAGNETIC TAPE?

ADVANTAGES

- LARGE STORAGE CAPACITY
- LOW COST
- REUSABLE (18,000 PASSES)
- RECORD/REPRODUCE SPEED
- STABILITY
- GOOD INTERCHANGEABLE MEDIA

DISADVANTAGES

- SERIAL ACCESS ONLY
- SLOW ACCESS COMPARED TO DISCS

ENVIRONMENTAL LIMITATIONS

- EASILY CONTAMINATED BY DIRT
- DETERIORATION OF OXIDE, BINDER, OR BASE MATERIAL WHEN EXCEEDING TEMPERATURE AND HUMIDITY RANGES:

TEMPERATURE RANGE	40° TO 90°F
HUMIDITY RANGE	20 TO 80%

2. Deterioration of oxide, binder or base
    a. Temperature
        1) Should remain as constant as possible ($\pm$ 5°F)
        2) Range of 40° to 90°F
            a) Brittle at lower temperatures
            b) Soft and stretches at higher temperatures
    b. Humidity
        1) Should be constant to within $\pm$ 10%
        2) Range of 20 to 80 %
            a) Lower humidity causes few problems
            b) Higher humidity causes binder between oxide and mylar to get sticky.

II-D REASONS FOR TAPE FAILURE

Tape failure may be caused by problems other than tape unit or electronic errors. Not meeting the critical physical requirements of tape or tape handling may be the cause of some tape errors. A minute section of tape, for instance, may lose its oxide coating. This dropout will cause the magnitude of the output to decrease significantly and may produce a tape error. The particle of oxide lost may be re-deposited elsewhere on the tape causing self contamination. This self contamination may cuase the tape to lift when passed over the head due to the double thickness of oxide, causing a second error.

Wrapping tension around the capstan and head assembly is also critical. Excessive tension may cause the tape to stretch or "take a set" if left in one position too long. It can also cause separation between the oxide and backing. This in turn alters the dimensions of tape causing instability as it is guided over the head. Low wrapping tension may allow the tape to lift off the head or allow tape to slip on the capstan.

Edge damage may be caused by improper tape storage, poor operator handling or scraping the edge of tape on some object in the transport. This damage may alter the tape width and allow it to "snake" over the head causing excessive dymanic skew.

A poor or unclean environment may decrease tape efficiency. Digital magnetic tape is susceptible to tape errors caused by minute particles of dirt. Poor atmosphere, unclean transport and not properly storing tapes are a few ways tape can become contaminated and unfit for use.

II-F SPECIFICATIONS

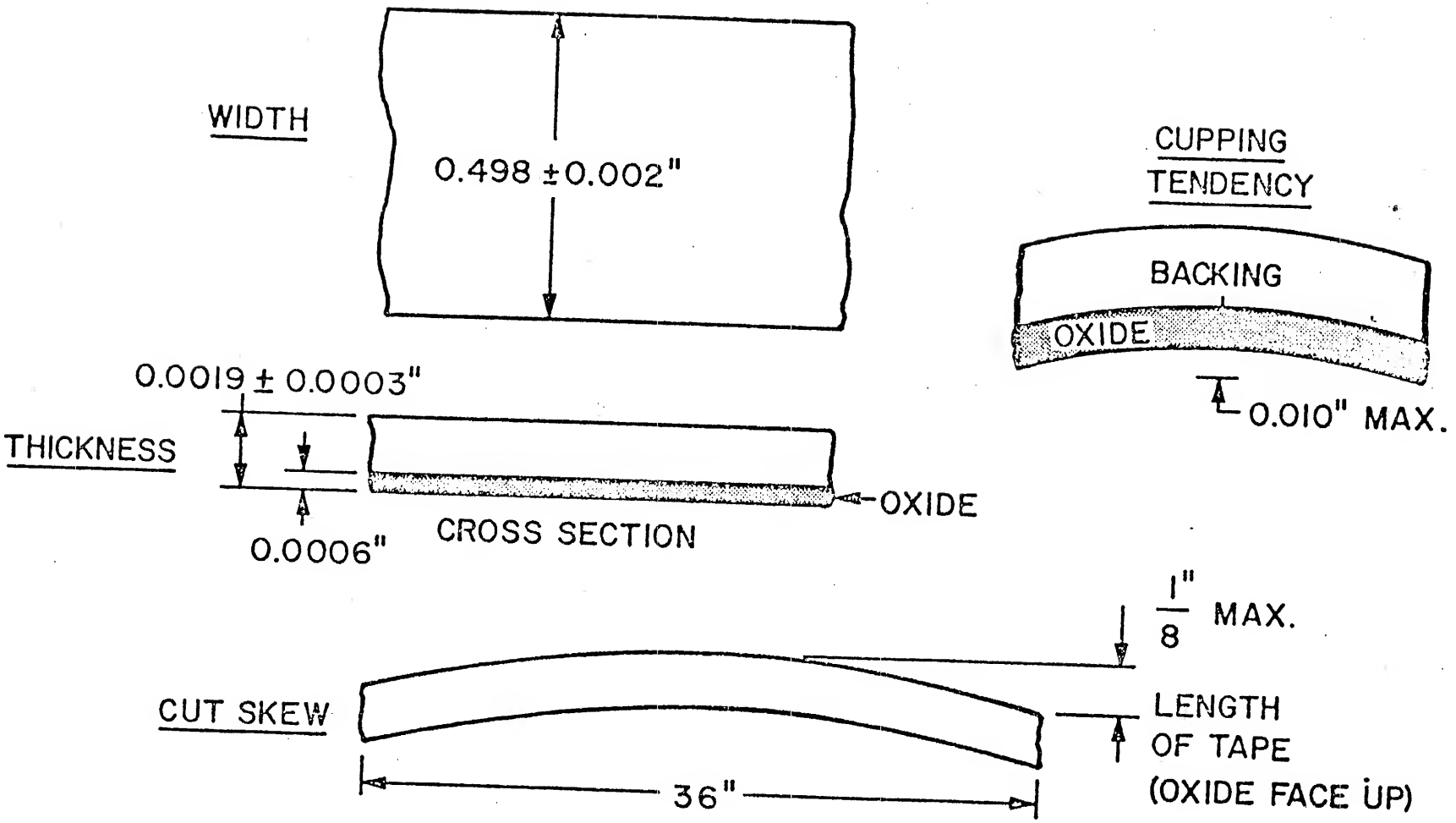
A major consideration of magnetic recording is the physical dimensions and tolerances of the recording media. Digital tape is typically 1/2 inch wide and 2 mils thick. The thickness is the sum total of 1-1/2 mil mylar backing and 1/2 mil oxide coating which is used to magnetically store data.

Longitudinal variations or cut skew is related to the way the original mylar sheet is cut and handled during the manufacturing process. The cross-sectional cupping tendency is caused by the difference in the co-efficient of expansion between the mylar and oxide coating.

REASONS FOR TAPE FAILURE

- DROPOUTS
- SELF CONTAMINATION
- LOW WRAPPING TENSION
- HIGH WRAPPING TENSION
- EDGE DAMAGE
- POOR ENVIRONMENT

TAPE


WIDTH
0.498 ±0.002"
CUPPING TENDENCY
BACKING
OXIDE
0.010" MAX.
0.0019 ± 0.0003"
THICKNESS
0.0006"
OXIDE
CROSS SECTION
1" / 8 MAX.
CUT SKEW
LENGTH OF TAPE (OXIDE FACE UP)
36"

NINE TRACK NUMBERING

ANSI TRACK NOS.	ASCII BIT DESIGNATIONS	IBM TRACK NOS.
1	b_3	5
2	b_1	7
3	b_5	3
4	P	P
5	b_6	2
6	b_7	1
7	Z	0
8	b_2	6
9	b_4	4

- NUMBERING BEGINS AT THE TOP OF THE TAPE WITH THE BOT MARKER TO THE RIGHT AND OXIDE SURFACE TOWARD VIEWER
- MOST SIGNIFICANT BITS ARE TOWARD CENTER OF TAPE
- IBM SCHEME HAS TRACK NUMBERING INVERTED TO ASCII BIT SIGNIFICANCE.

Design of a digital tape transport must take all physical characteristics of tape into consideration in order to pass it accurately over the head assembly.

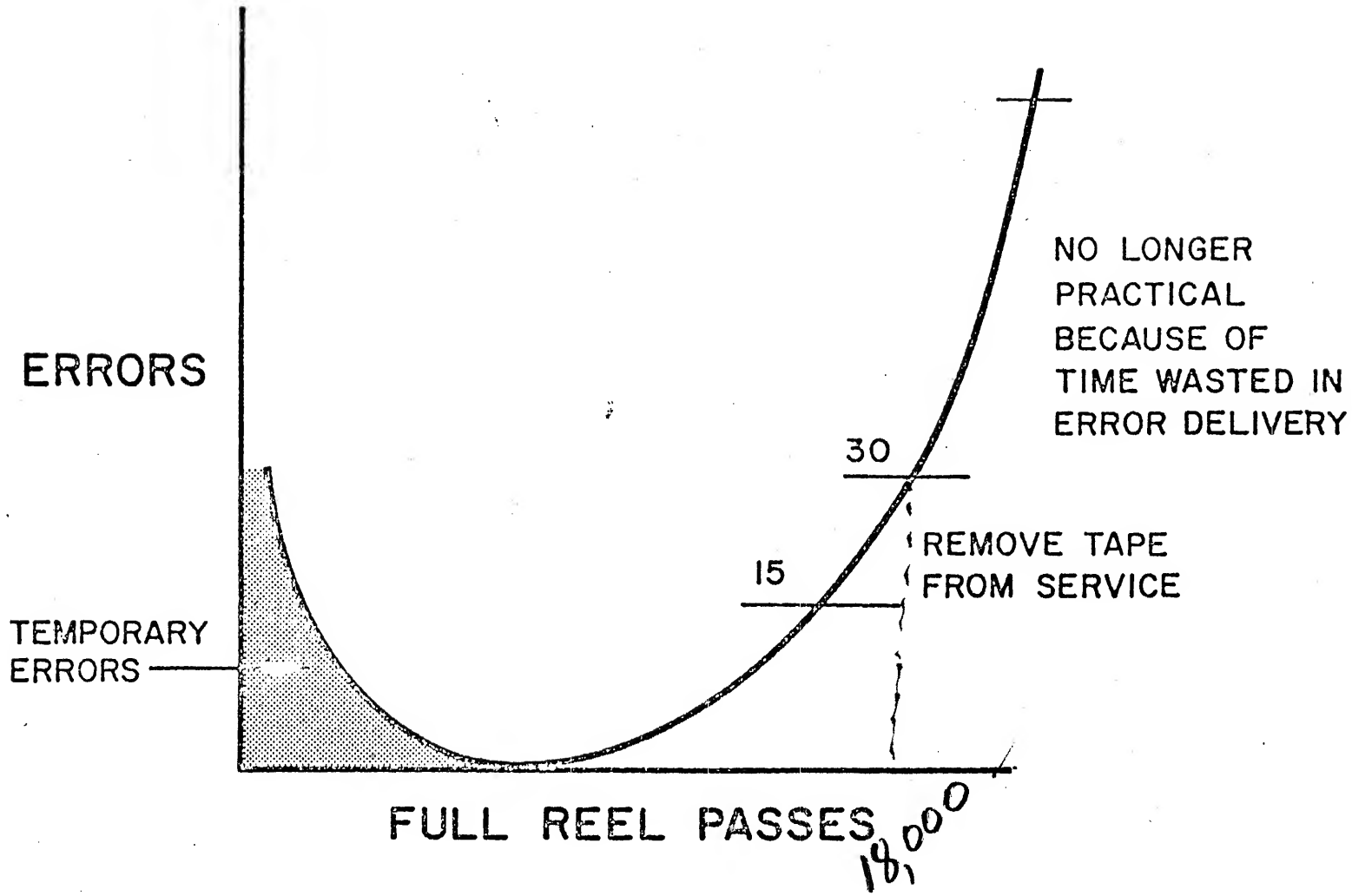
Errors are more likely to occur at the edge of the tape than near the center. This is true because tape skew problems and edge damage effect the outer tracks to a greater extent than the inner tracks.

II-H MAGNETIC TAPE LIFE

A new reel of magnetic tape may exhibit a number of temporary errors due to dirt or imperfections in the oxide coating. Passing the tape over a tape cleaner or head a few times cleans or polishes the tape and achieves optimum performance.

After some number of passes over the head, a tape may begin to exhibit an excessive number of errors. When a user experiences some number of errors (typically 15 to 30), the tape is no longer economical for use. At this time the tape is removed from service to be cleaned and verified. If this is not successful, the front or used portion of tape must be removed and a new load point tab installed.

MAGNETIC TAPE PERFORMANCE



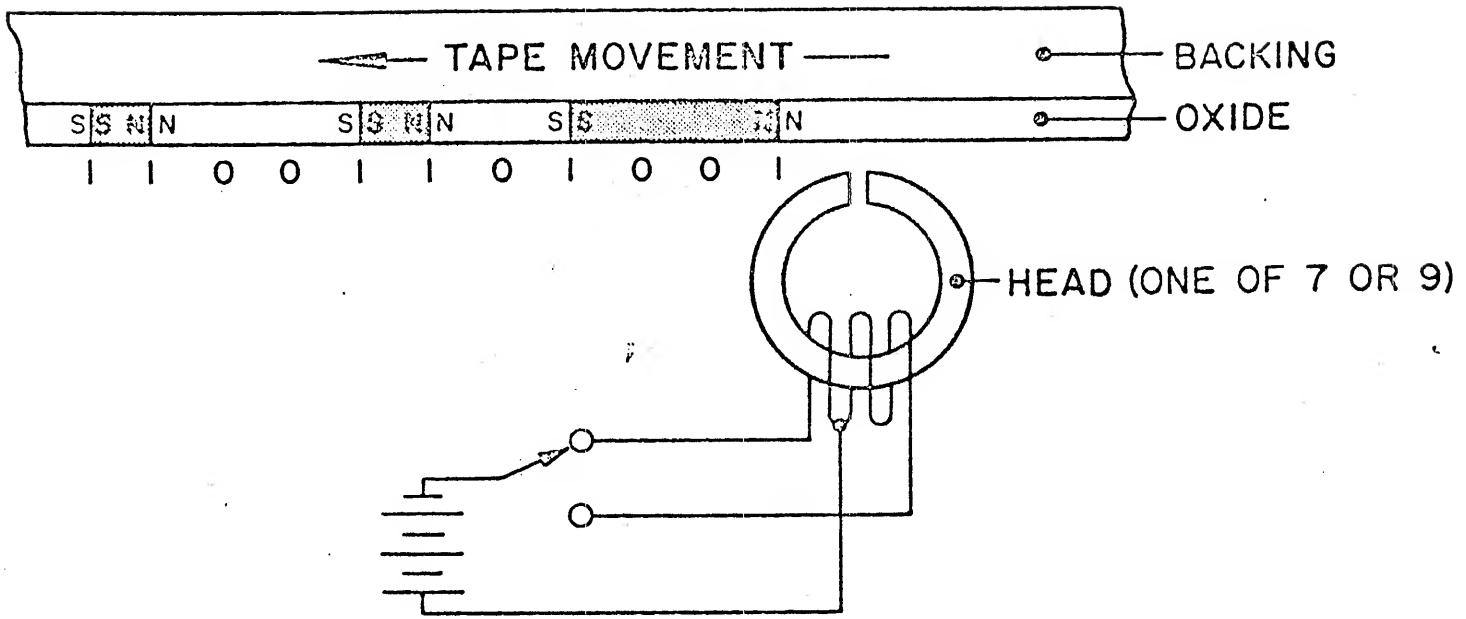
III NRZI RECORDING

The method most used for recording digital magnetic tape is called Non Return to Zero Invert (NRZI). NRZI represents a logic one by inverting the magnetic saturation of the oxide. That is, NRZI recording is accomplished by a change in flux to write a "one" and no change in flux to write a "zero".

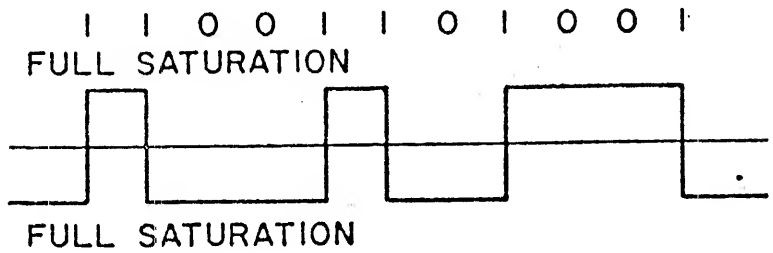
As tape passes over the head assembly it first contacts the erase head which magnetically saturates it to the reset flux state. After passing over the erase head it then contacts the write stack which saturates each track separately starting at the beginning of the record in the reset flux state. Each logical one in a track then inverts the magnetic saturation causing a concentration of flux at that point.

The tape output is used to generate a read clock. For "0" locations it is necessary to write a "1" in at least one channel each bit time. In nine track tape drives, odd parity is used for lateral error checking. Thus, if the tape unit is provided with an all zeros byte (8 bits of data) the parity circuits will generate a "one" bit in the ninth channel.

NRZI RECORDING

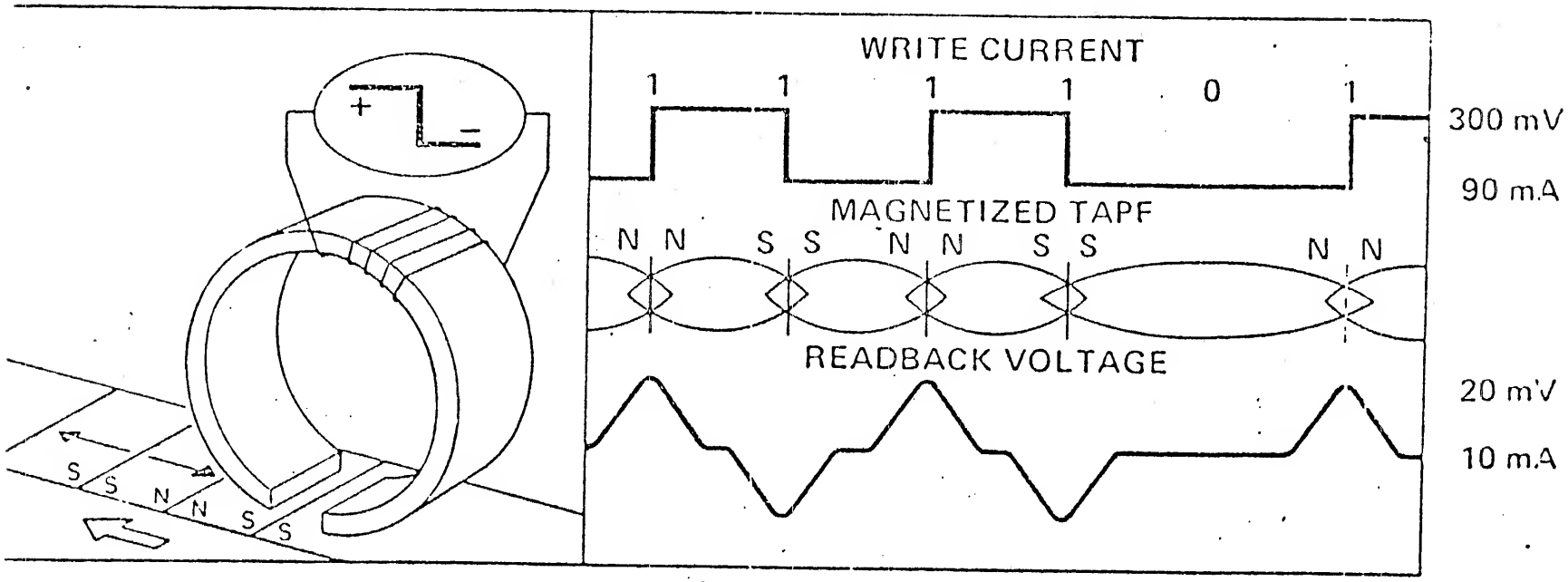


OPERATION OF THE SWITCH. ONLY A CHANGE FOR A LOGICAL "ONE" NO CHANGE IN FLUX FOR A LOGICAL "ZERO."



THE RECORDING PROCESS

DATA IS RECORDED ON TAPE AS IT PASSES A HEAD WHICH IS POLARIZED IN EITHER A NORTH OR SOUTH DIRECTION



III-B TAPE FORMAT

A. Industry compatibility

If digital tapes are to be interchanged between tape units, standards of industry compatibility must be observed. Five basic requirements of compatibility are:

1. Physical dimensions and magnetic properties of the tape being used.
2. The format of the data records being stored on tape.
3. The density or characters per inch at which data is being recorded.
4. The method of magnetically representing data bits on tape.
5. The coding format of the data characters being stored on tape.

USA standards have provided guidelines covering all aspects of digital recording that must be observed if interchangeability is a product goal.

B. Format

Tape format is a consideration of industry compatibility. It establishes standards for placement of the load point (beginning of tape) and EOT (END OF TAPE) reflective tabs; first record placement, and inter-record gap size.

The load point tab is placed on the reference (operator) edge of the mylar side of tape, approximately 20 feet from the physical beginning of tape. The first record begins no less than 1/2 inch from the trailing edge of the load point tab (IBM specifications). Record length is dependent on software. However, standards suggest record length be between 18 and 2048 characters. The inter-record gap (IRG) for a nine track system is nominally 0.6 inch.

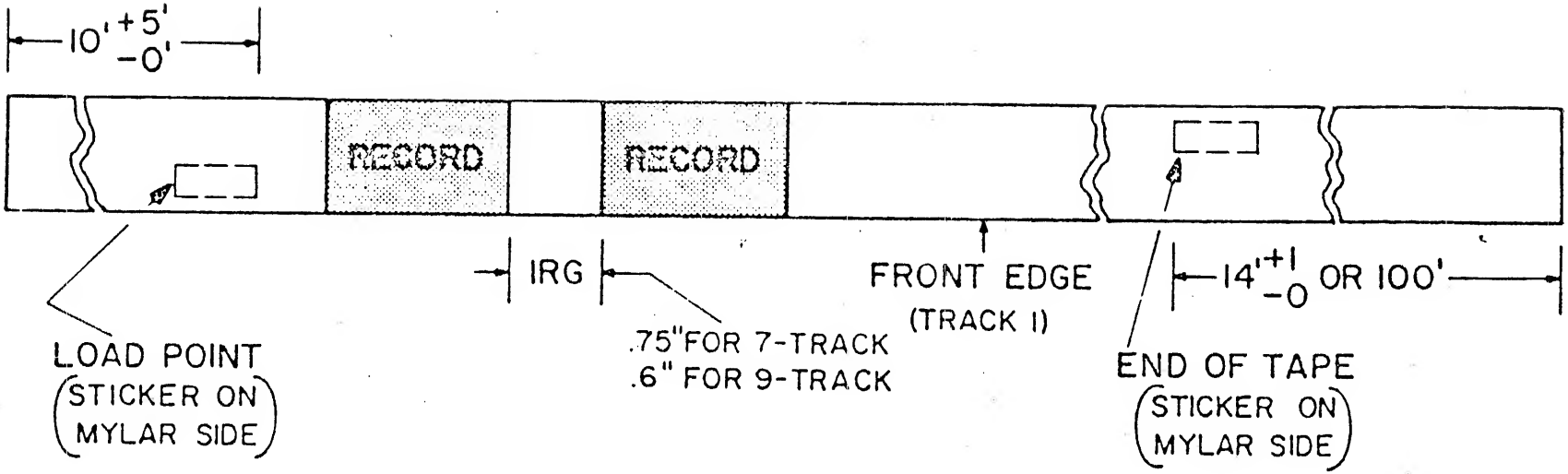
The end of tape reflective tab is placed on the transport (back) edge of the mylar side of tape approximately 14 feet from the physical end of tape. This tab is used to signal the end of tape is near.

B drives have an IRG of 0.67 in. and E drives have IRG of 0.62 in.

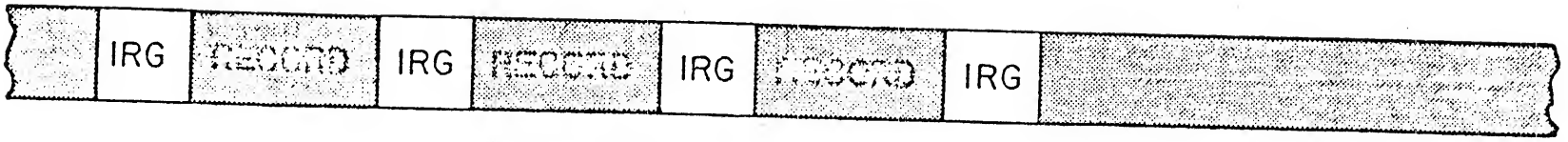
C. Records

Recording format is defined by the programmer and the capabilities of the computer/controller. The single record format employs one logical record followed by an inter-record gap. These records may be either fixed or variable length.

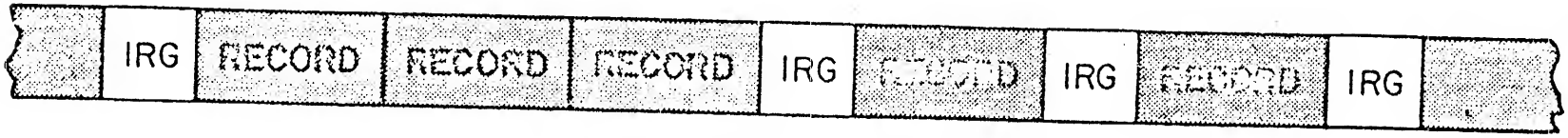
TAPE FORMAT


10' +5' -0'
RECORD
RECORD
IRG
.75" FOR 7-TRACK
.6" FOR 9-TRACK
FRONT EDGE
(TRACK 1)
14' +1 -0 OR 100'
LOAD POINT
(STICKER ON MYLAR SIDE)
END OF TAPE
(STICKER ON MYLAR SIDE)

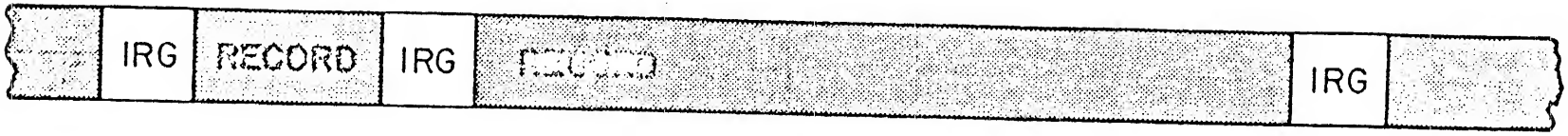
RECORDS



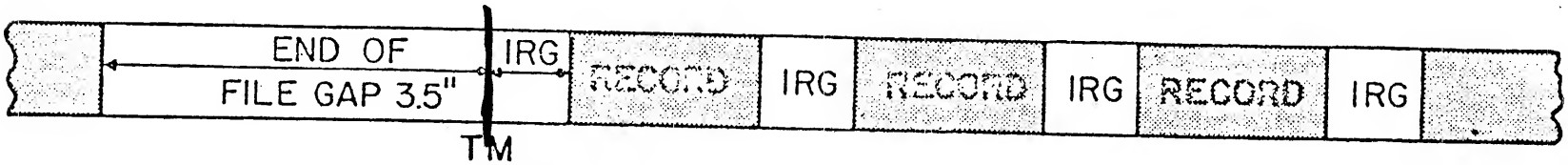
SINGLE RECORDS



BLOCKED RECORDS



VARIABLE LENGTH RECORDS



TAPE MARK (FILE MARK)
WITH A FILE GAP

Blocked records merge two or more logical records into one long block. Each individual record within the block is separated by a unique character.

A tape mark (file mark) is a one character record used by software to indicate the logical end of a file or group of records. It's format consists of a single character followed by a check character called a longitudinal redundancy check character. The tape mark is normally preceded by a 3 to 4 inch gap of erased tape although the gap is not a requirement.

III-C PARITY

1. Lateral Parity

Lateral (or vertical) parity checking is a method of detecting read or write errors. Seven track character format uses even or odd lateral parity depending on application. However, when using even parity 7 track format, each character including a data blank must be coded. A blank must be a coded character rather than a blank space on tape. Odd parity is typically used for scientific applications and even parity is used for commercial data processing applications. Nine track tape units always employ odd lateral parity.

2. CRCC

Nine track tape units employ odd lateral parity checking, logitudinal parity checking and cyclic redundancy checking. The Cyclic Redundancy Check Character (CRCC) is a one character representation of all bytes in a data record. It is developed by exclusive-"ORing", each byte with a shifted CRC register. The result is a character that somewhat represents a diagonal parity check character which is written 4 character times after the ~~LRCC.~~ RECORD The LRCC is then written 4 character times after the CRCC.

The 7970 generates the CRCC but does not test it.

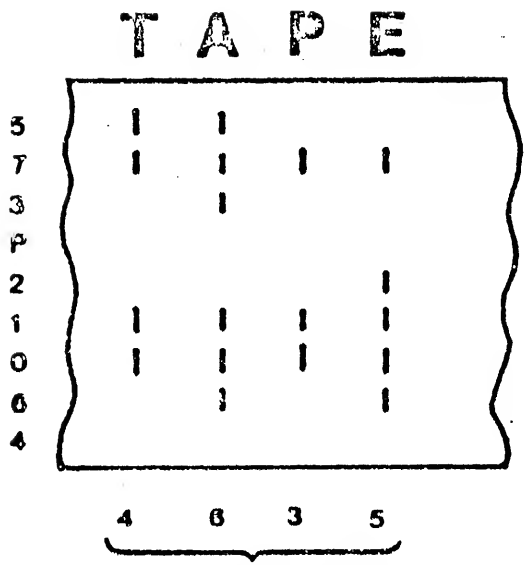
Channel scrambling is performed in the 7970 to maintain industry compatibility. The purpose of channel scrambling is to place the most used channels on the center of tape, which decreases the possibility of tape error.

3. Longitudinal Parity

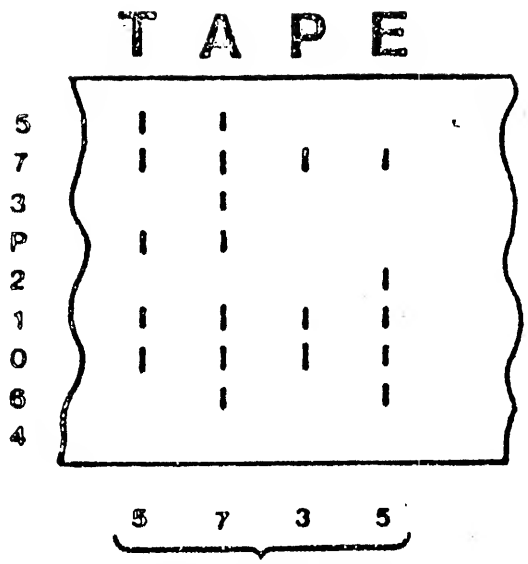
Longitudinal parity is maintained by the use of the LRCC (Longitudinal Redundancy Check Character). The LRCC is written on tape 4 character times after the CRCC and maintains even longitudinal parity per track in each record. It is written by returning all write heads to the reset flux state.

Lateral parity is not maintained on the LRCC although the 9 track LRCC will always be odd parity. This is because of the formulation of a Cyclic Redundancy Check (CRC) character.

LATERAL PARITY

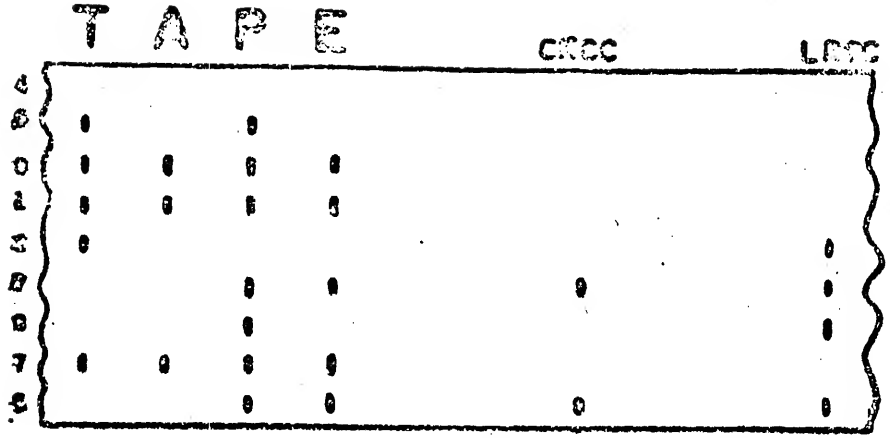


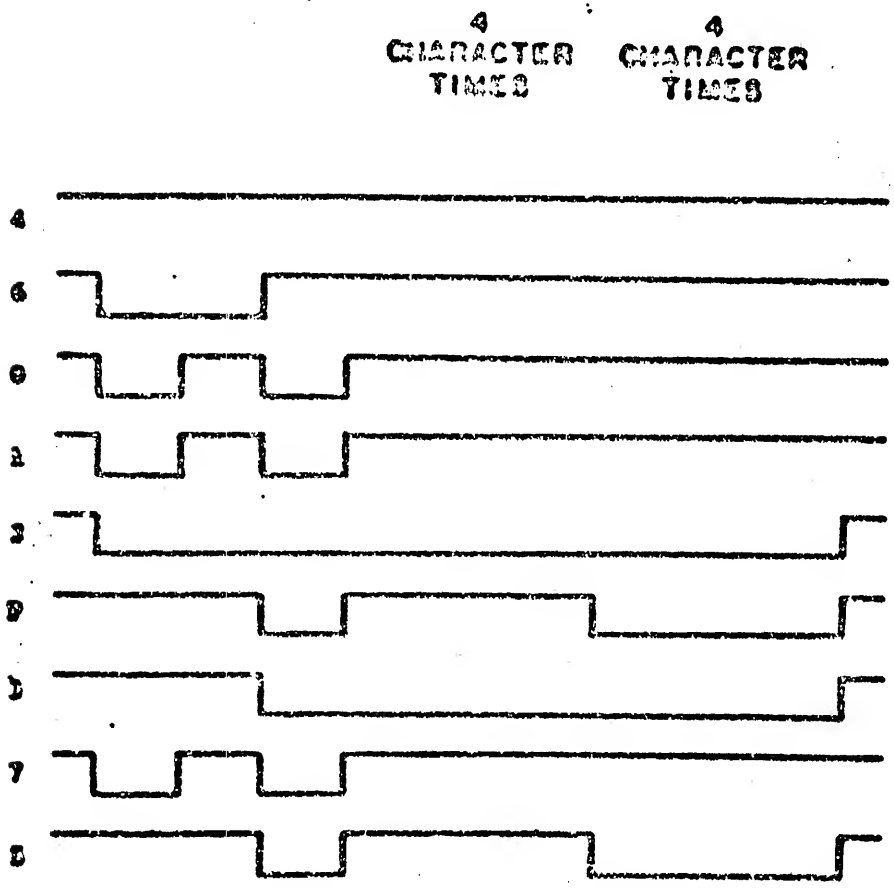
LATERAL BIT COUNT
SOME EVEN, SOME ODD



ALL ODD. BY ADDING
THE PARITY BIT

9 TRACK ERROR CHECK





CRCC REGISTRATION

INPUT REGISTER	OE	CRCR POSITION	OE	CRCR POSITION	CRCR CHANGED
P	OE	7			P
0	OE	P			0
1	OE	0			1
2	OE	1	OE	7	2
3	OE	2	OE	7	3
4	OE	3	OE	7	4
5	OE	4	OE	7	5
6	OE	5			6
7	OE	6			7

4. Error Correction Philosophy P.E.

Error correction circuits provide the ability to correct the majority of errors encountered in normal tape operations. Tape control error correction assumes that the data on tape was written correctly and any errors detected are a result of tape damage or read failure. No attempt is made to correct the tape. Correction is performed only on the data sent to the channel interface. Corrected bytes are automatically checked to be sure the correction is done properly.

Not all errors are correctable. Error correction circuits can correct almost any combination of errors as long as they all occur in the same track within a nine-track block. If a block contains errors in more than one track, they cannot be corrected. The key to error correction is determination of which track contains the errors. Once the track in error has been located, actual correction becomes a simple matter.

III-D Records on Tape

5. Density

There are three common bit densities for NRZI digital magnetic recording. They are 200, 556 and 800 bits per inch (BPI), Bit-to-bit spacing therefore ranges between 0.005 and 0.00125 inches.

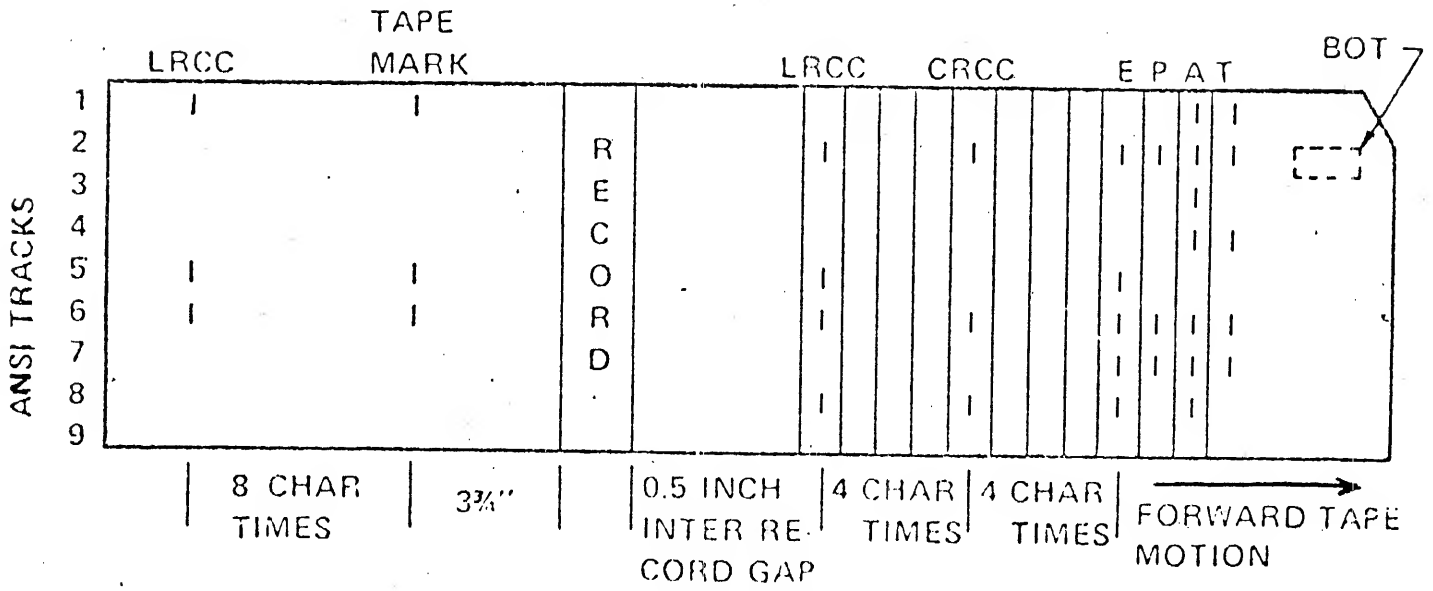
Most NRZI HP tape drives record at 800 BPI. However, HP does provide options for the other two densities.

The bit spacing for PE drives can be either 0.000625 in, or 0.000312 in. The spacing of 0.000312 in. exists when either all ones or all zeros occur. It is the difference between a data bit and a phase transition (See VIII-A). The data bit-to-bit spacing is 0.000625 in.

NRZI tape is capable of storing about 23 megabytes of data on one reel of tape. Typically it is more like 15 megabytes due to IRG, check characters etc.

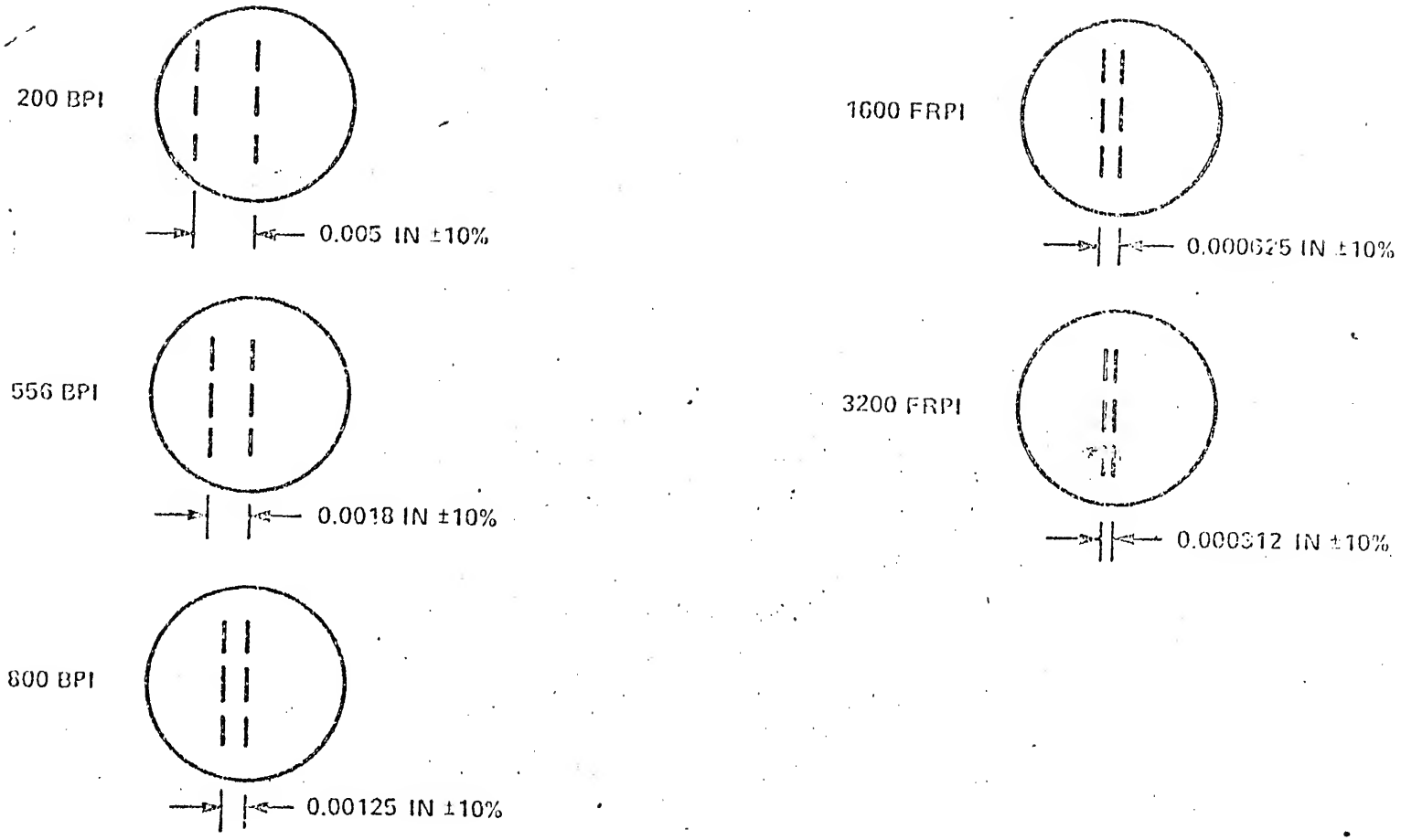
PE is about twice these amounts.

NINE TRACK 800 CPI NRZI FORMAT



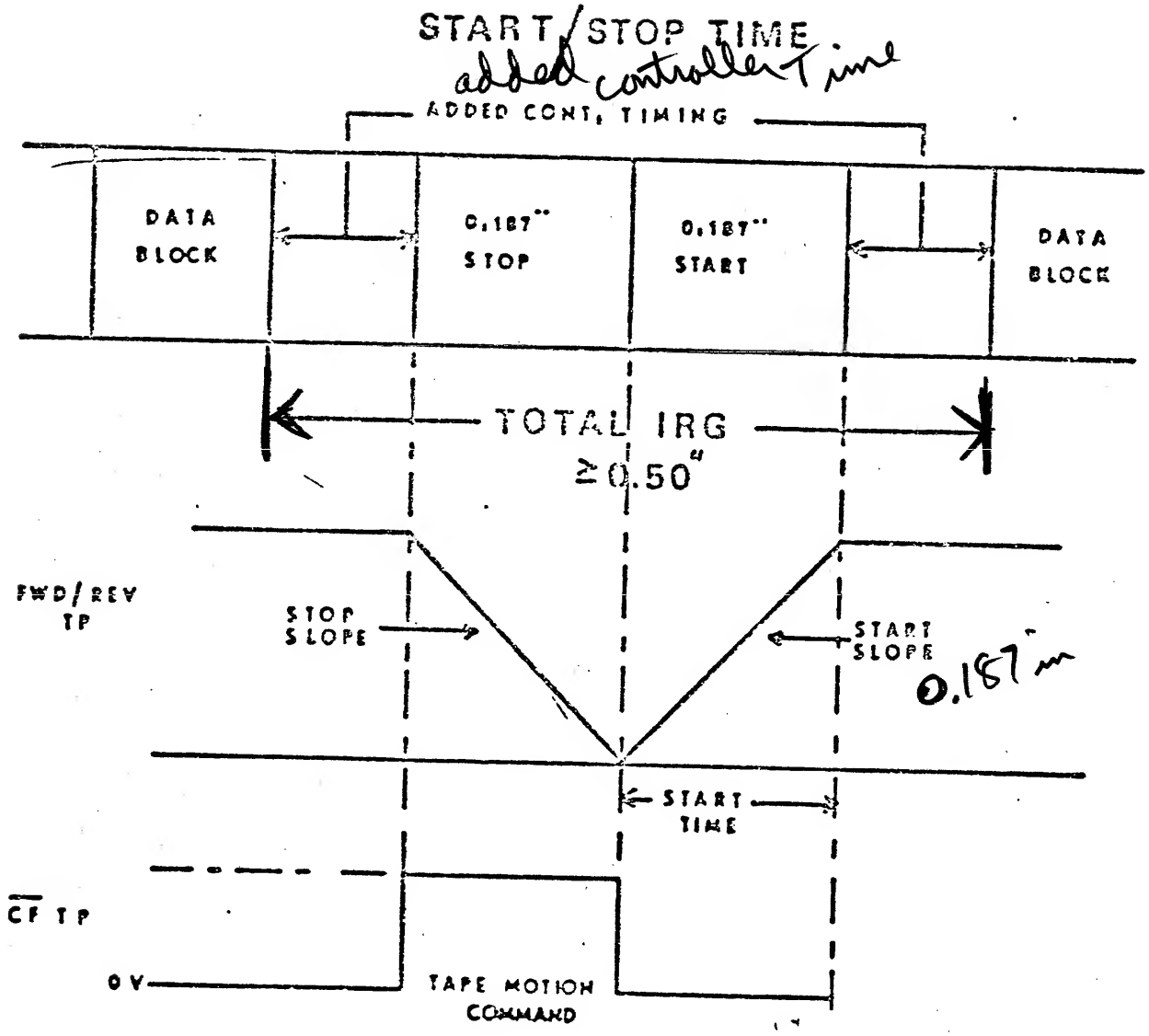
- ONE BYTE PER CHARACTER ON TAPE
- ALL NINE-TRACK OPERATIONS USE ODD VERTICAL (LATERAL) PARITY
- TRACK WIDTH .043 INCH
- SPACING .055 INCH CENTER TO CENTER

RECORDING DENSITY



III-E Start/Stop (Ramp) Time

The tape unit is specified to ramp the tape up to synchronous tape speed, and ramp it down to a complete stop in a very precise distance of 0.187 ± 020 inches. If the tape unit stop/start distance is in error when writing a tape, the tape IRG (Inter-Record-Gap) distance will be in error. Data can also be undetected when reading a previously recorded correctly formatted tape if the tape unit stop/start distance is in error. Because the start and stop ramp distances are both 0.187, the total ramp up and ramp down distance is 0.374 inches. The tape unit controller timing must add to this stop/start distance, the timing necessary to make a total correct length of the IRG of greater than 0.50 inches. The distance tape travels is a product of tape speed and time (TS x Time = d). Hence the ramp distance can be measured as a function of time for a given tape speed. Stop/Start time and distance can be determined by observing the ramp time on the capstan PCA.


START/STOP TIME
added controller Time
ADDED CONT. TIMING
DATA BLOCK
0.187" STOP
0.187" START
DATA BLOCK
TOTAL IRG
≥0.50"
FWD/REV TP
STOP SLOPE
START SLOPE
0.187"
START TIME
CF TP
0 V
TAPE MOTION COMMAND

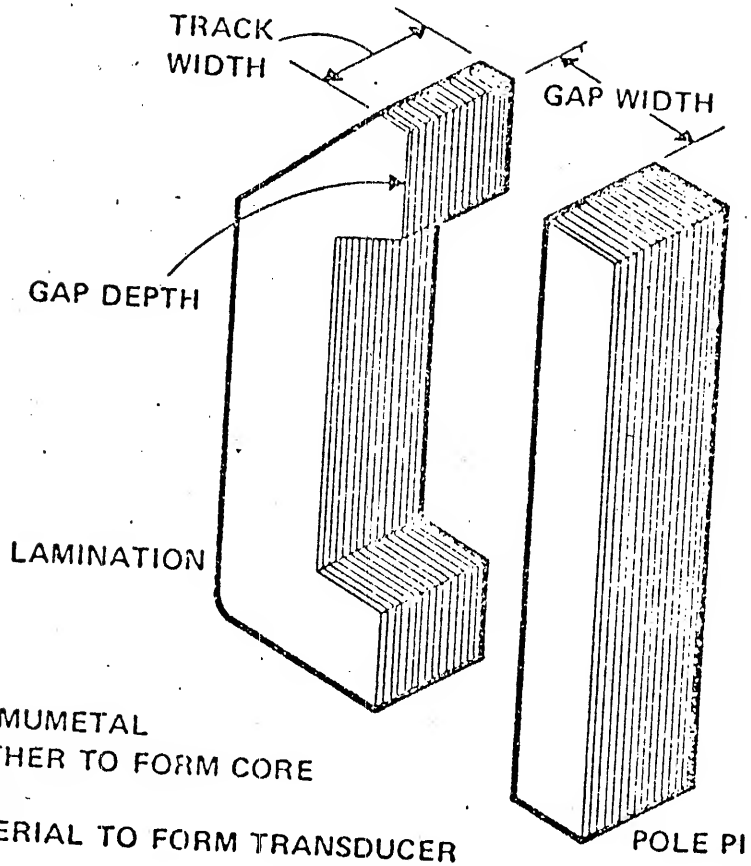
Since accurate tape guiding over the read/write head is imperative, all components in the head assembly tape path are mounted on a base plate. Tape guiding through the head area is accomplished by two tape guides. The edges of the tape are contacted by two ceramic washers, one fixed position (reference) and one spring loaded to allow for slight variations in tape width. In the forward direction, tape first contacts a slotted tape cleaner which scrapes any foreign articles from the tape prior to its reaching the head stacks. Tape then contacts a full width, high density erase head used to saturate tape in the reset flux state. After contacting the erase head it reaches first the write head stack then the read stack. A head gate near (but not contacting) the tape and over the read/write stack is used to reduce write to read stack crosstalk. A laminated intra-stack shield is placed between the stacks to further reduce the crosstalk. Each track in the head assembly has its own laminated read and write pole, including a coil winding and read/write gap. Separating the tracks are intra-pole shields to eliminate channel to channel crosstalk. As the tape passes over the write head it is magnetically saturated at the write gap. As it passes over the read head, a change in flux polarity induces a current in the read coil which is transmitted to the read electronics.

As a head wears, the smooth curve flattens on the top forming a porch . If the porch reaches the edge of the pole, read or write errors may result. At this time the head may be refurbished or re-contoured. This may be accomplished only once since the re-contouring extracts approximately 0.005 inches from the total surface.

Wear grooves are cut into the read/write stacks at the point where the tape edges contact the stack. Their purpose is to decrease tape edge curl due to uneven wear across the head.

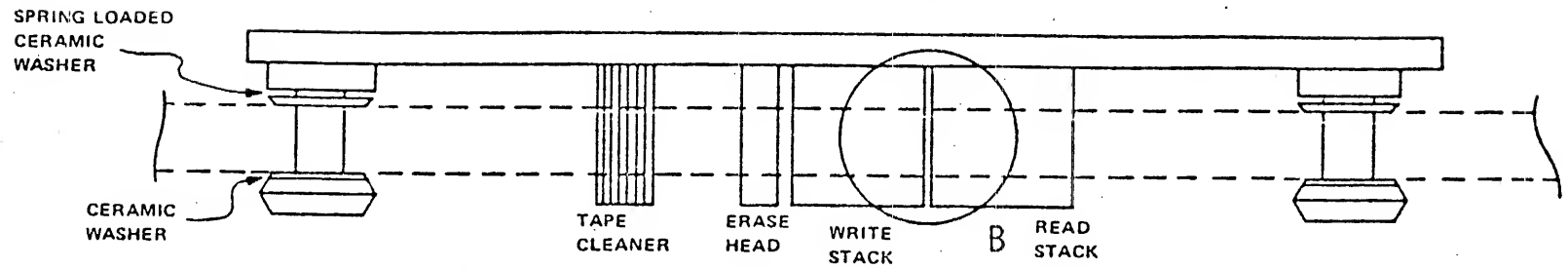
The wrap angle around the head stacks, erase head, and tape cleaner is extremely critical. Any alteration of the position of a component may cause characteristic changes in the entire head assembly.

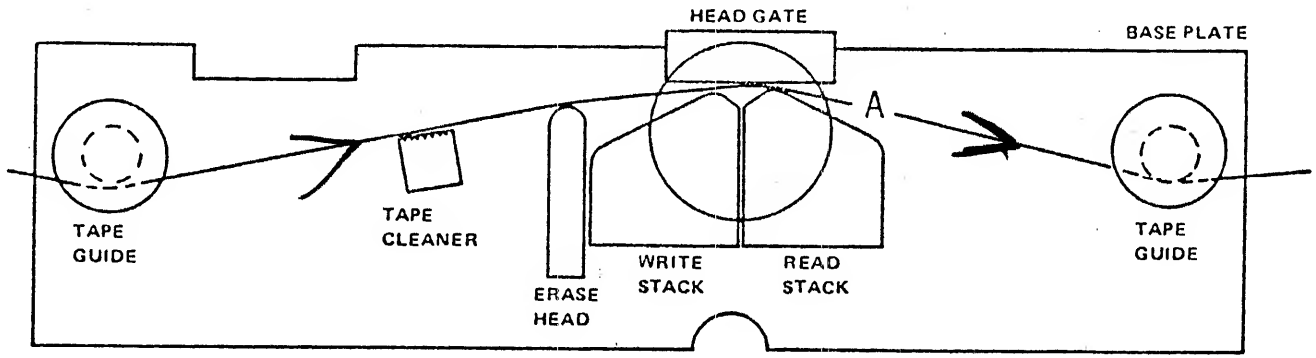
HEAD CONSTRUCTION

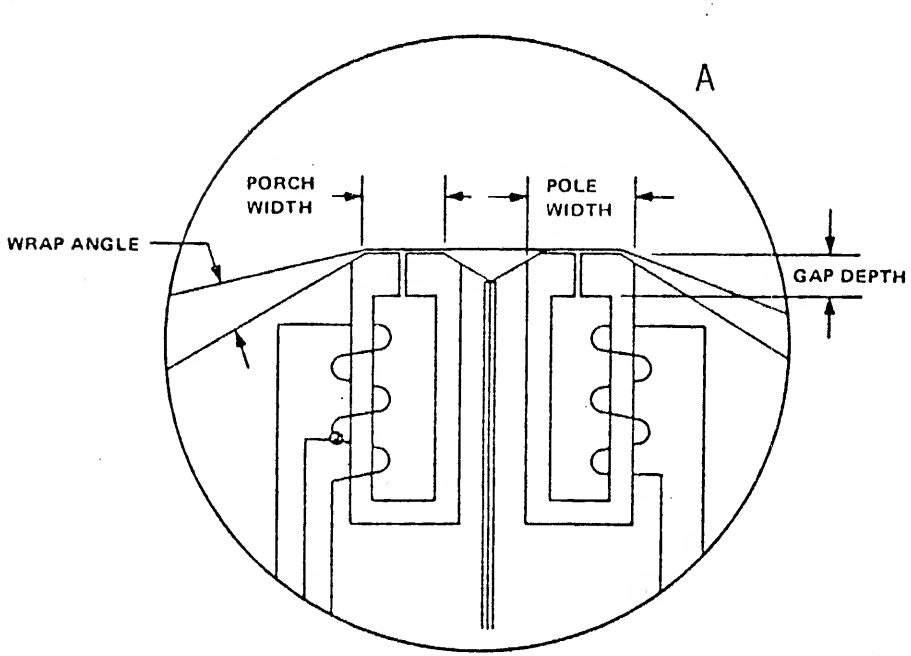


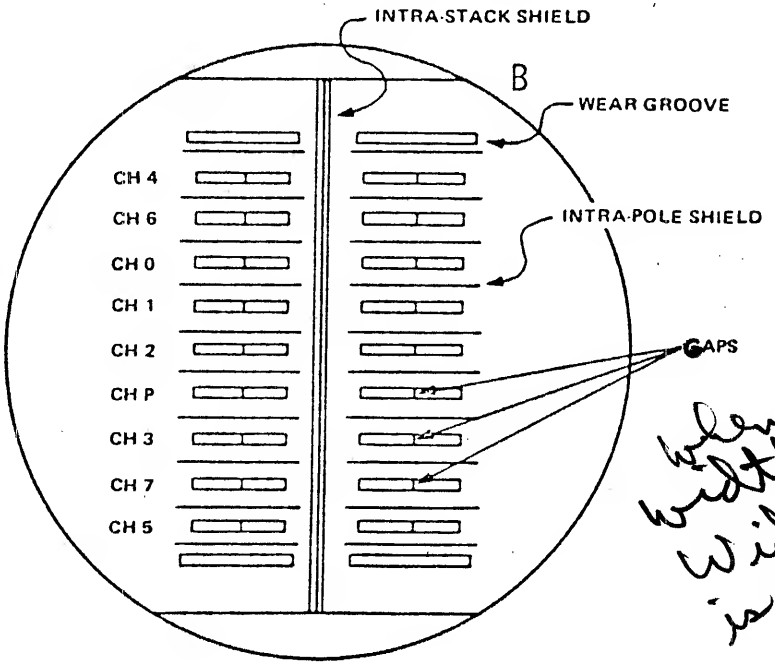
- FRETS ARE ETCHED FROM MUMETAL
- FRETS ARE BONDED TOGETHER TO FORM CORE
- CORE IS WOUND WITH COIL
- ASSEMBLED WITH GAP MATERIAL TO FORM TRANSDUCER

HEAD ASSEMBLY (9 TRACK, ERASE, READ, WRITE)









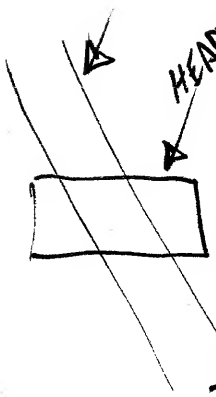
when porch width = pole width head is ideal

IV-B Gap Scatter

Gap scatter is a measure applied to the tolerances which prevent either 7 or 9 tranducers from being perfectly aligned. In spite of the fact that the tranducers are optically aligned the drying epoxy pushes the transducers out of line because of its differential drying action. This gap scatter is generally a parabolic contour. Standards in use today specify that gap scatter is less than 120 microinches. Some manufacturers specify gap scatter as low as 80 microinches. Aside from the problem of eliminating gap scatter during the production process, gap scatter produces problems in attempting to record bits of data on tape that are perfectly aligned.

IV-C Skew

When a digital magnetic tape head stack is constructed, slight variations may occur in gap alignment. Consider the misalignment (called gap scatter) of read gaps. As tape passes over the head the character (assuming good bit alignment) contacts the read gaps at different times depending on gap scatter. This time differential is called static skew.



Static skew is the angular error between the axis of the tape and the head gap line. It is the result of manufacturing.

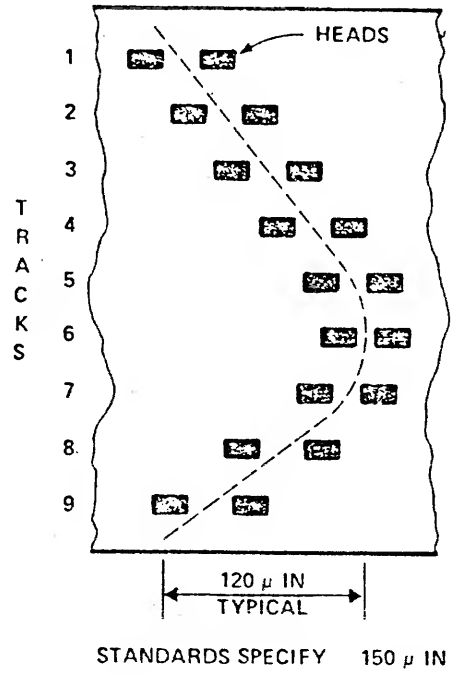
To compensate for the effects of static skew, the outputs from the read head are presented to skew delay circuits. These delay circuits are adjustable and are used to electrically align all data bits of a character.

Dynamic skew is a variable angular error between the head gap-line and the horizontal axis of the tape. It is caused by friction in the tape path. Any component in the tape path can contribute to total dynamic skew. Some examples follow:

1) Tape-edge damage
2) Head assembly worn or damaged
3) Guides poorly aligned or damaged
4) Capstan assembly worn or damaged

correcting these problems will reduce or eliminate dynamic skew.

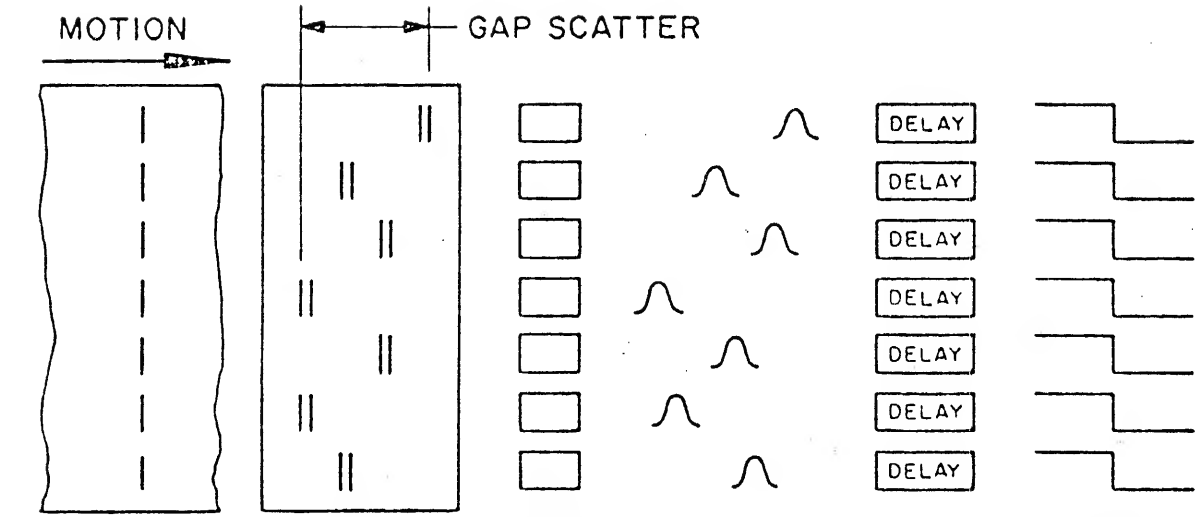
GAP SCATTER



STANDARDS SPECIFY 150 μ IN

- THE DRYING EPOXY PUSHES HEAD TRANSDUCERS OUT OF LINE RESULTING IN BITS BEING DISPLACED ACROSS TAPE
- GAP SCATTER HAS PARABOLIC CONTOUR

STATIC SKEW
(GAP SCATTER)

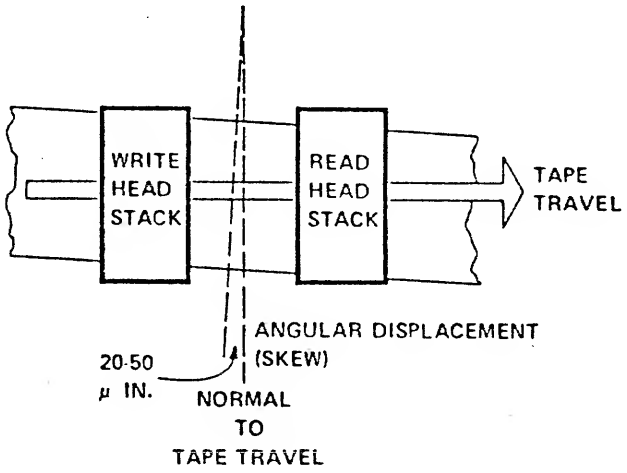


- TWO DELAY ADJUSTMENTS FOR EACH TRACK
- POTENTIAMETER ADJUSTMENT RATHER THAN DELAY TAPS

TAPE SKEW

IS THE ANGULAR DISPLACEMENT FROM THE NORMAL TO TAPE TRAVEL AS DETERMINED BY

- TAPE SLITTING TOLERANCES
- TAPE GUIDE ALIGNMENT TOLERANCES



IV-D Pulse Crowding

Pulse crowding is the name of an effect which occurs during the record and reproduce processes. When flux transitions at a given rate are recorded and reproduced they tend to be pushed together. When the transition rate changes to a lower rate, the last pulse at the high frequency tends to drift out in time. Certain data patterns will cause shifts of a bit cell of a hundred microinches or more. This effect is most pronounced at 800 characters per inch using the NRZI code. Since a random pattern using 1600 cpi phase encoding results in only 2 fundamental frequencies the problem of pulse crowding is greatly reduced. This fact is inherent in hardware. In spite of attempts to minimize the effect, some tape transports become known as "data pattern" sensitive.

IV-E Write Time Asymmetry

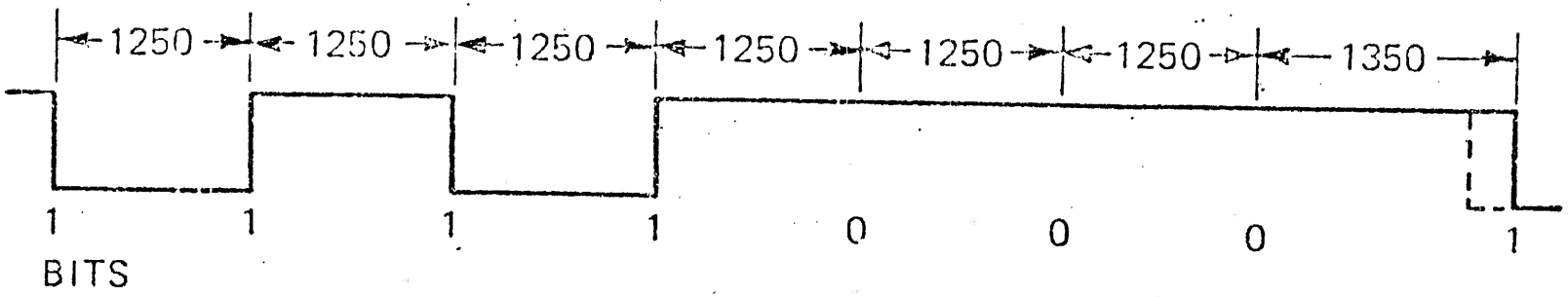
The coil on the head is actually a center-tap coil. Current flowing in one half will produce a flux in one direction while current flowing in the other half will produce a flux in the opposite direction. This switching action cannot be perfectly balanced because of the impedance variation between the two different halves of the coil. The ideal spacing between bits shown in the accompanying figure, therefore,will be modified. The spacing between every other bit can be accurately set to conform to the 2500 microinch spacing; however, the intervening bit which is written by the other half of the coil will have a tolerance variation of $\pm$ 38 microinches. The exact amount of the variation as well as the direction can be measured on any specific head, but because the shift takes place on every other bit, compensation is not possible.

IV-F Summary of Four Problems

The effect of the four problems, previously described, on individual bit displacements is shown in the table. In spite of the fact that initially the theoretical spacing between pulse flux transitions was 1250 microinches, one can see that total displacement may vary on individual tracks up to 1/3 of the total distance. To help compensate for these inherent problems, a number of techniques either mechanical or electrical have been designed to overcome or circumvent the problems.

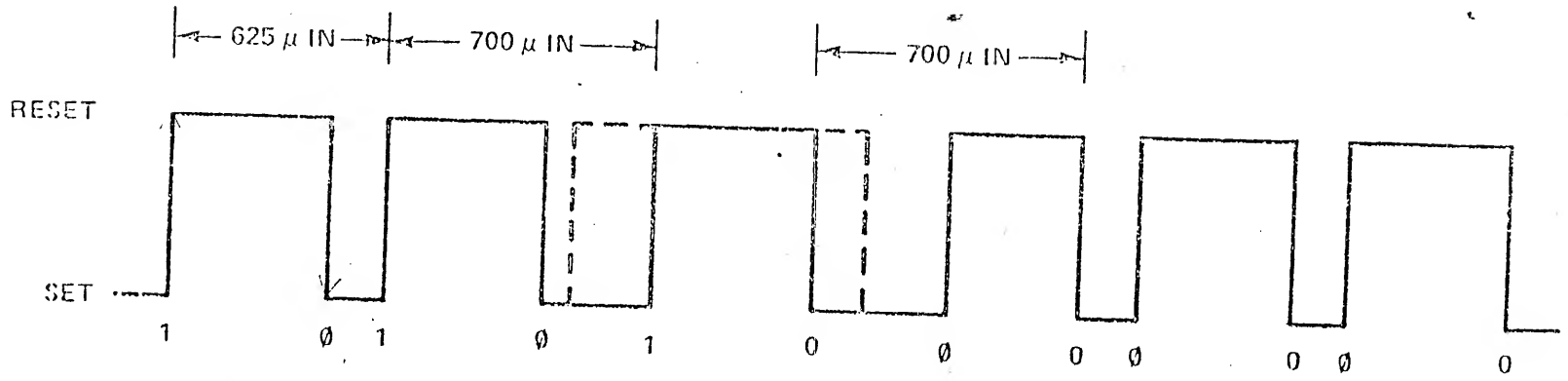
NRZI PULSE CROWDING

- INTERACTION OF RESONANT MAGNETIC FIELDS TENDS TO BUNCH FLUX TRANSITIONS ON TAPE
- WRITING CERTAIN DATA PATTERNS CAN CAUSE SHIFTS UP TO 100 μ IN
- MOST PRONOUNCED EFFECTS AT 800 CPI
- PHASE-ENCODED 1600 CPI LIMITS THE PROBLEM

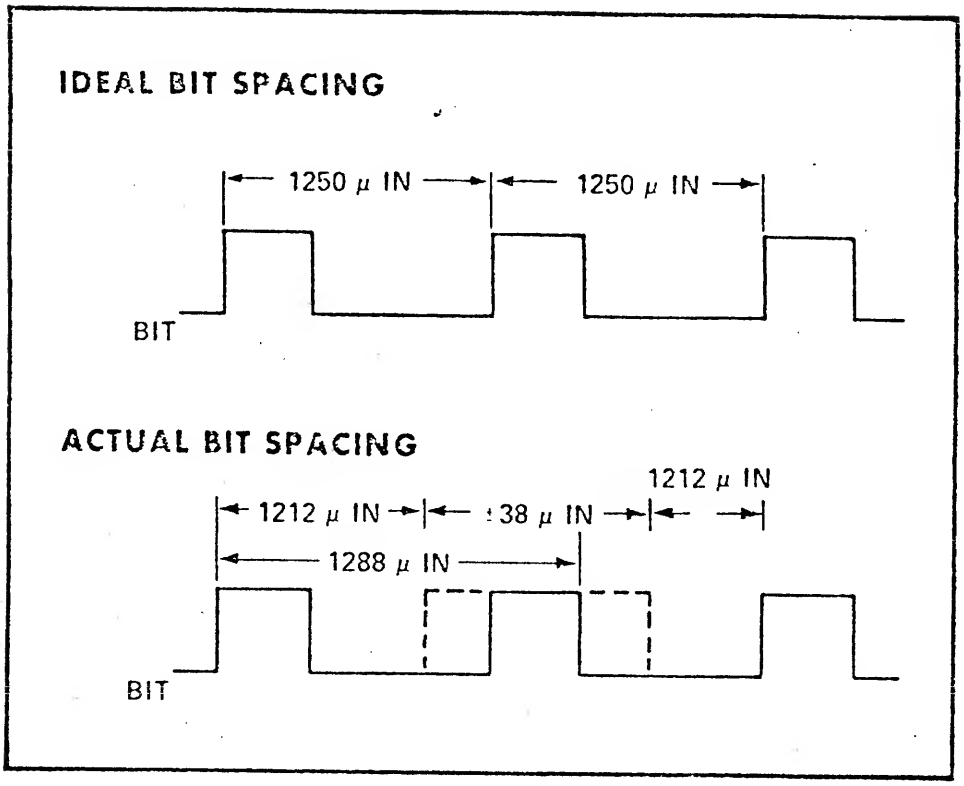


PE PULSE CROWDING

- INTERACTION OF MAGNETIC FIELDS TENDS TO BUNCH FLUX TRANSITIONS ON TAPE
- WRITING CERTAIN DATA PATTERNS CAN CAUSE SHIFTS UP TO 100 μ IN.
- MOST PRONOUNCED EFFECTS AT 800 CPI
- PHASE-ENCODED 1600 CPI LIMITS THE PROBLEM



WRITE TIME ASYMMETRY



SUMMARY OF FOUR PROBLEMS

PROBLEM	TYPICAL ERROR	EFFECTIVE ON		TOTAL * POSSIBLE
		WRITE	READ	
GAP SCATTER	120 μ IN	YES	YES	240 μ IN
TAPE SKEW	50 μ IN	YES	YES	100 μ IN
WRITE TIME ASYMMETRY	75 μ IN	YES	NO	75 μ IN
PULSE CROWDING	50 μ IN	YES	YES	100 μ IN
				515 μ IN**

*THIS MEASURE IS TO BE TAKEN FOR ILLUSTRATION PURPOSES ONLY

**APPROXIMATELY 1/3 OF DISTANCE BETWEEN RECORDED BITS

V-A NRZI simplified Overall Block Diagram

The overall simplified block diagram of the 7970 Tape Unit functionally represents the transport read electronics, write electronics, and interface or controller.

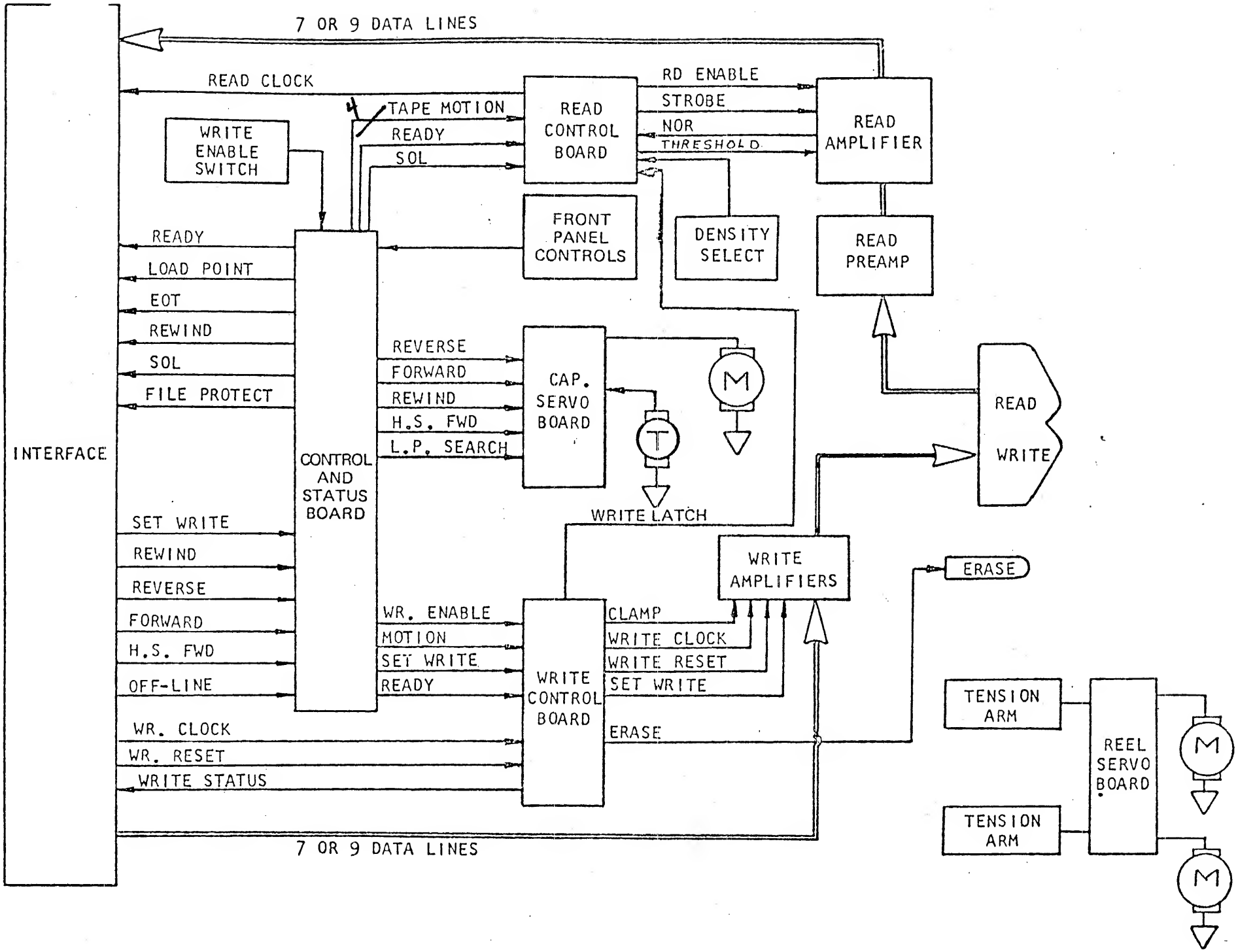
Note that all motion and status (except write status) lines enter or leave the control/status PC board. This is the heart of the 7970 transport which controls tape motion. All tape motion is provided by the capstan and its associated servo control. Tape storage is provided by the reel servo system. Mass tape storage is handled by the reels and low volume immediate access storage is provided by tension arm assemblies. Reel motion is controlled by photosense assemblies mounted on the tension arms which provide input to the reel servo relative to the position of the tension arms.

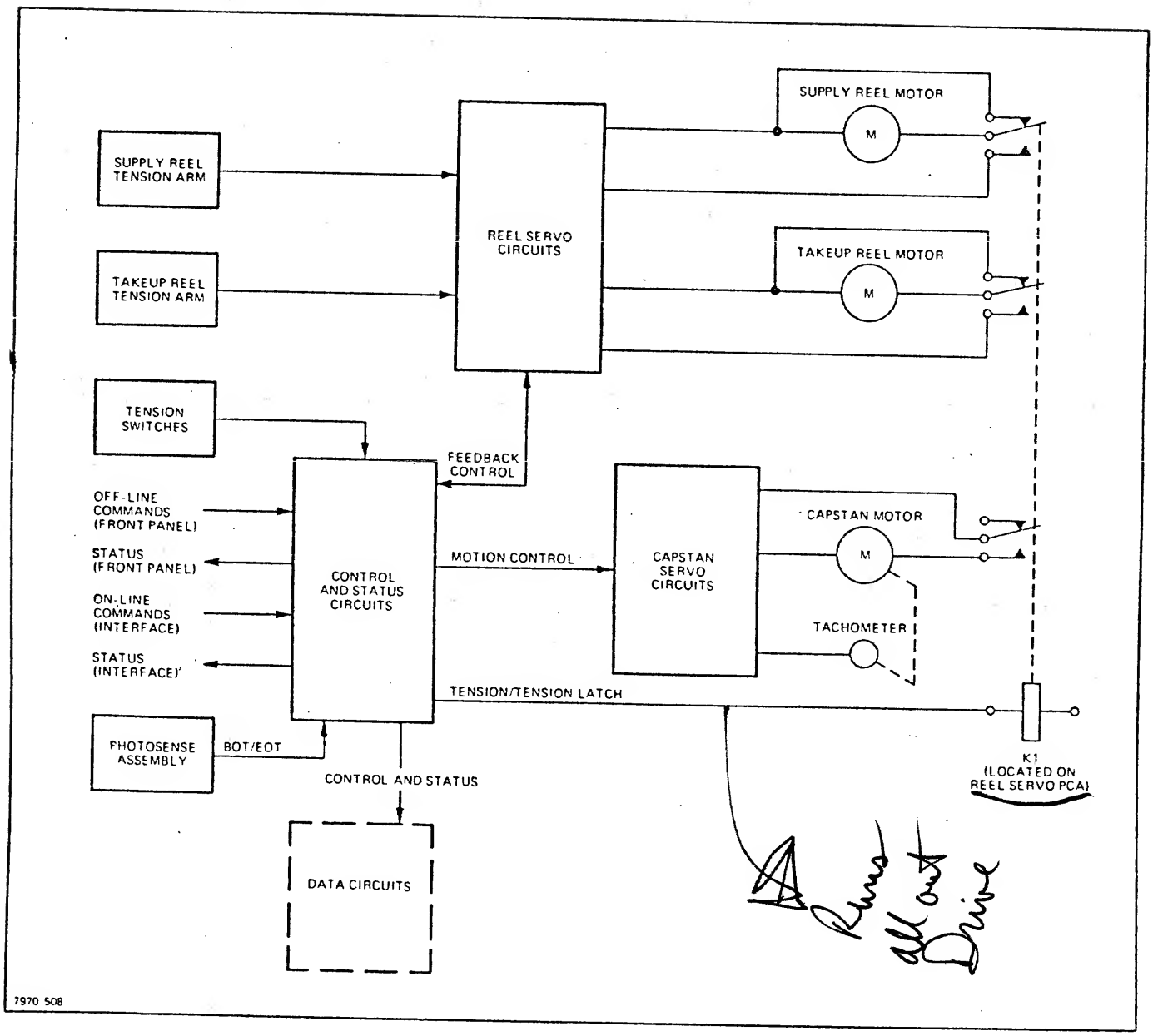
The write electronics circuits are controlled by the combined effort of the control/status board and the direct input from the interface. Data is received by the write amplifiers directly from the interface. The read electronics circuits are controlled by the control/status board. During a read operation, data is presented to the interface along with a read clock for interface timing.

V-B Simplified Tape Movement Electronics

The tape transport controls the movement of magnetic tape, provides power for read and write data circuits, and supplies status signals to the interface. Off-line commands (Reset, Rewind, Load, and On-Line) are initiated by front panel switches. On-line commands (High-speed, Reverse, Forward, Rewind, and Off-Line) are generated by the interface. The off-line and on-line commands are processed by the control and status circuits and result in controlling signals for the capstan servo, reel servo, and data circuits. Status signals for the interface and front panel indicators are also provided by the control and status circuits.

At initial power on, the capstan motor circuit is open, and the reel servo motors are shorted. When the load switch is depressed the tension command is initiated. At the same time the capstan motor and reel motor circuits are completed.


7 OR 9 DATA LINES
READ CLOCK
TAPE MOTION
READY
SOL
WRITE ENABLE SWITCH
READ CONTROL BOARD
RD ENABLE
STROBE
NOR
THRESHOLD
READ AMPLIFIER
FRONT PANEL CONTROLS
DENSITY SELECT
READ PREAMP
READY
LOAD POINT
EOT
REWIND
SOL
FILE PROTECT
INTERFACE
CONTROL AND STATUS BOARD
REVERSE
FORWARD
REWIND
H.S. FWD
L.P. SEARCH
CAP. SERVO BOARD
M
T
READ
WRITE
WRITE LATCH
SET WRITE
REWIND
REVERSE
FORWARD
H.S. FWD
OFF-LINE
WR. ENABLE
MOTION
SET WRITE
READY
WRITE CONTROL BOARD
WRITE AMPLIFIERS
ERASE
CLAMP
WRITE CLOCK
WRITE RESET
SET WRITE
ERASE
WR. CLOCK
WR. RESET
WRITE STATUS
TENSION ARM
TENSION ARM
REEL SERVO BOARD
M
M
7 OR 9 DATA LINES



Tape Transport Functional Block Diagram

When tape tension is established the tension arms swing away from the tension limit switches. With tape tensioned, the capstan and reel motor returns are maintained. When the LOAD switch is released, the control and status circuits initiate a load point search. During load point search, the reel servo circuit operates with voltage feedback and the capstan servo pulls tape forward at 20 IPS.

When the load point tab is detected by the photosense assembly, the control and status circuits terminate the load point search, and tape motion stops. The control and status circuits provide a load point status to the interface, and the front panel LOAD indicator illuminates.

Pressing the ON-LINE switch establishes interface control of the tape unit. At that time, except for RESET, the front panel controls have no control of the tape unit. Depressing RESET releases the interface control and allows front panel control of the tape unit. Depressing REWIND rewinds the tape onto the supply reel, should the tape break or run off the reel, tension arms would open the limit switches at the extreme ends of the tension arm swing. This would break the capstan motor circuit and short the reel motors providing dynamic braking of the reel motors.

V-C Power Supply

The power supply voltages can be divided into two major sections: the unregulated, and the regulated voltages. Primary input power must be 115 or 230 volts ± 10% at 48 to 66 Hz. Maximum power requirement is 400 VA at high line.

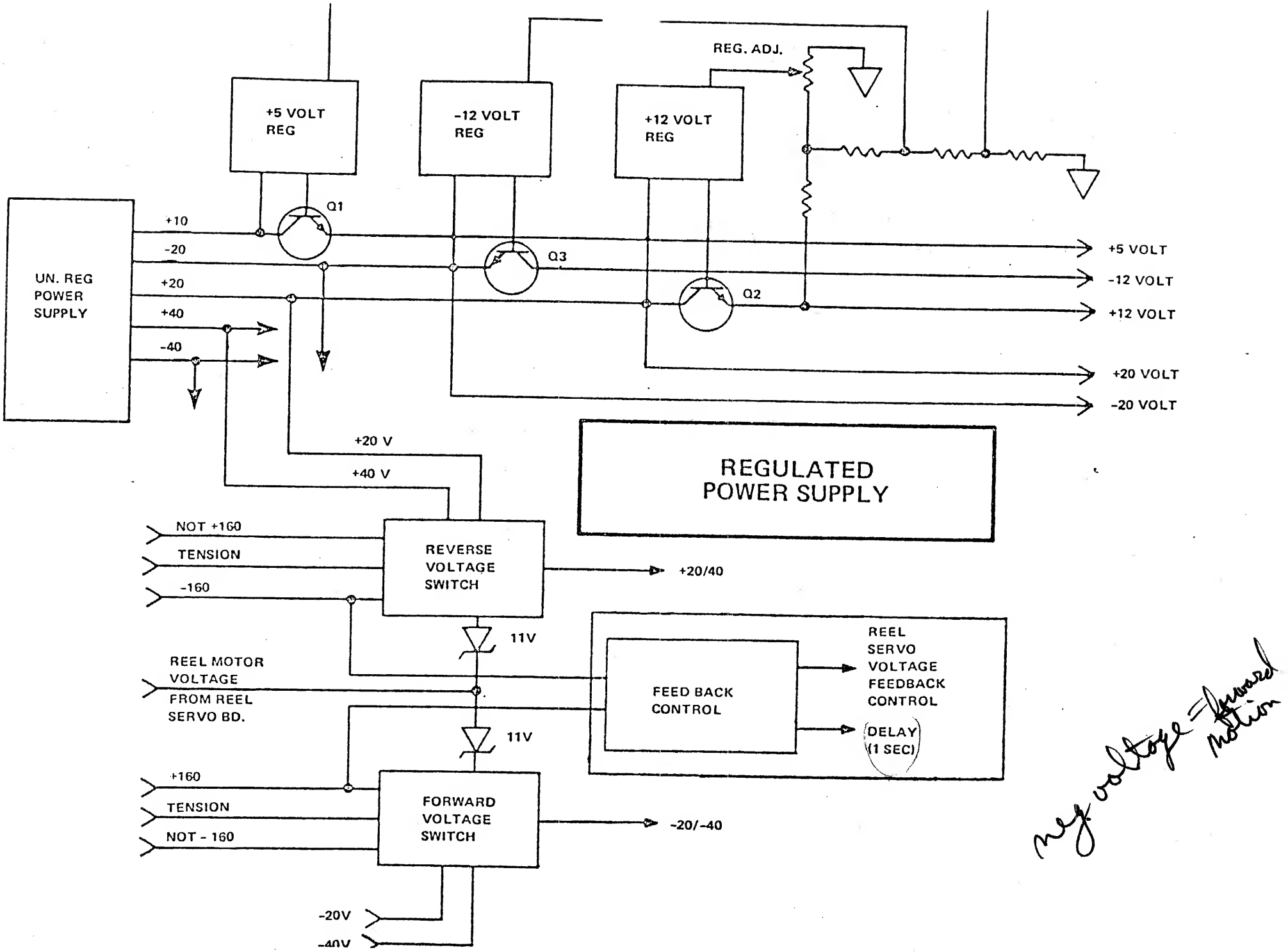
Output from 3 diode bridge networks in the unregulated power supply provide ± 40 volts for the reel servo, ± 20 volts, and + 10 volts. The unregulated + 20 volts supplies the + 12 volt regulator which employs adjustable feedback for varying the output level. This output goes throughout the transport for utility use as well as to a voltage divider network on the regulator board. Taps from the voltage divider network are fed to the - 12 and + 5 volt regulator as a reference voltage. Consequently, as the + 12 volt output is varied, the -12 and + 5 volt outputs also vary.

During high speed operations the voltage switch on the regulator monitors the reel servo motor voltage. If the voltage from the servo amplifier exceeds 11 volts (indicating that the tension arm swing is approaching its limits) the voltage switch turns on, supplying 40 volts to the appropriate amplifier. Once the motor voltage returns to less than 11 volts, the voltage switch turns off and removes the 40 volt supply.

The feedback control circuit presents a signal to the reel servo board that causes the reel servos to operate on voltage feedback during normal operations and allows current feedback for high speed operations.

The 1 second delay is provided to prevent a false tape brake from being sensed when going from High Speed Forward or High Speed Reverse to another tape motion mode.

The primary circuit of the power supply transformer includes a switch that allows selection of 115 or 230 Vac operation, a power on-off switch, and a line filter/power connector.


REG. ADJ.
+5 VOLT REG
-12 VOLT REG
+12 VOLT REG
Q1
Q3
Q2
UN. REG POWER SUPPLY
+10
-20
+20
+40
-40
+5 VOLT
-12 VOLT
+12 VOLT
+20 VOLT
-20 VOLT
+20 V
+40 V
REGULATED POWER SUPPLY
NOT +160
TENSION
-160
REVERSE VOLTAGE SWITCH
+20/40
11V
REEL MOTOR VOLTAGE FROM REEL SERVO BD.
FEED BACK CONTROL
REEL SERVO VOLTAGE FEEDBACK CONTROL
DELAY (1 SEC)
11V
+160
TENSION
NOT - 160
FORWARD VOLTAGE SWITCH
-20/-40
-20V
-40V
neg voltage = forward motion

When 115 Vac power is selected, the two primary windings of the power transformer are in parallel and fuse F1 provides overload protection. When 230 Vac power is selected the two primary windings of the power transformer are in series, and fuse F2 is placed in series with the primary winding to provide overload protection.

Diodes CR3 and CR4 of the power distribution PCA are for protection in the event a short circuit takes place between the plus and minus 22.5 dc lines (on the reel servo for instance). They prevent any possibility of reversal of the + 5, + 12, and - 12 volt dc polarity caused by the type of short mentioned.

The heat sink-mounted power transistors are on the power distribution PCA. The 7970E power distribution PCA has additional transistors to provide more current drive for the + 5 volt output. (NRZI drives do not require the higher current).

The power regulator PCA contains regulator circuits for the + 5, + 12, and - 12 volt outputs. It also contains the reel servo voltage switching circuit and delay circuit.

The + 12 volt regulator uses an integrated circuit voltage regulator with an internal temperature compensated voltage reference. Regulation is obtained by dividing the output voltage (R3, R4, and R5) and comparing the divided voltage with the internal reference. The output voltage of the + 12 volt regulator is adjustable by variable resistor R4. Series regulator transistor Q2 (located on the heatsink external to the regulator) is protected by current limiting. The current foldback knee is set to approximately 2.8 amperes by R1 and R2. Short circuit current is set to approximately 1.3 amperes by current sense resistors R7 and R8 located on the heatsink external to the regulator).

The + 12 volt regulator has the only adjustment for all three regulators. The variable resistor R4 is adjusted to establish the value of the + 5 volt supply. When the + 5 volt output is adjusted to its correct value, the $\pm$ 12 volt regulators will also be adjusted correctly. The test points for + 5, + 12, and - 12 volts are located on the power regulator PCA.

The -12 volt regulator uses an integrated circuit voltage regulator. The reference for the -12 volt regulator is derived from the regulated +12 volt source. Current limiting of the -12 volt regulator is set at 1.2 amperes as determined by R9.

The +5 volt regulator uses an integrated circuit voltage regulator. The reference for the +5 regulator is the +12 volt regulator output using R23, R25, and R26. Current limit of the +5 volt regulator is approximately 4.0 amperes (8.0 amperes on 7970E) controlled by current sense resistor R6, located external of the regulator on a heatsink. In the event of an over-voltage condition, silicon controlled rectifier CR1 conducts and shorts the +5 volt supply. The 4 ampere short circuit current will blow fuse F5 which is in series with the +10 volt unregulated supply.

When the high speed logic inputs from the control and status PCA are present the output of Q18 switches the reel servo amplifier to high gain. As the drive signal at the output of the servo amplifier reaches a sufficient amplitude to break down CR4 and CR6 (REV or FWD) the plus or minus 20 VDC is switched to plus or minus 40 VDC. (plus = Reverse, minus = forward).

During a high-speed reverse operation (rewind), the HSREV signal from the control and status circuits is gated with the tension signal. When either tension arm deflects enough both reel motors approach full RPM. When the motor voltage exceeds the breakdown voltage of CR4 (approx 11V) the condition established by the gating of the HSREV and TENSION signals allows current through CR4 to forward bias Q5. Transistors Q6 and Q7 conduct placing 40V on the 20/40 volt line.

During a high-speed forward operation, the voltage switching circuits function the same as in the fast reverse operation except that CR6 is used instead of CR4. The HSFWD signal is gated with the Tension signal to allow motor voltage to switch the -40 volt switch (Q12/Q13).

The delay circuit is located on the power regulator printed-circuit assembly. The delay circuit provides an additional one-second delay following the end of a high-speed command. The one-second delay prevents further motion commands from the interface from being processed during the one-second period. The one-second delay is also used to switch the reel servo operating mode from high gain back to normal. The switching takes place after reels are slowed.

During normal operation, U5A-3 and U5B-4 are at zero volts. A HSREV or HSFWD signal from the control and status circuits will put sufficient. positive voltage on the base of Q15 to turn it on. Base current for Q15 is supplied by R28 or R29. When Q15 conducts capacitor C8 immediately discharges through Q15 causing Q16 and Q18 to be cut off. Feedback control to the reel servo changes from approximately +8 volts to approximately -8 volts. The negative potential also reverse biases Q17 and the delay output line switches to +5 volts.

When the high-speed command (HSFWD or HSREV signal) is removed and Q15 loses base current, capacitor C8 is then charged through R33 (one-second time constant). When C8 is charged to +5V, Q16 and Q18 conduct and the feed-back control changes from -8V to +8V. The delay output switches to 0 volts.

Transistor Q17 has a high failure rate. The symptoms are that the unit won't go into load point, usually after high speed rewind.

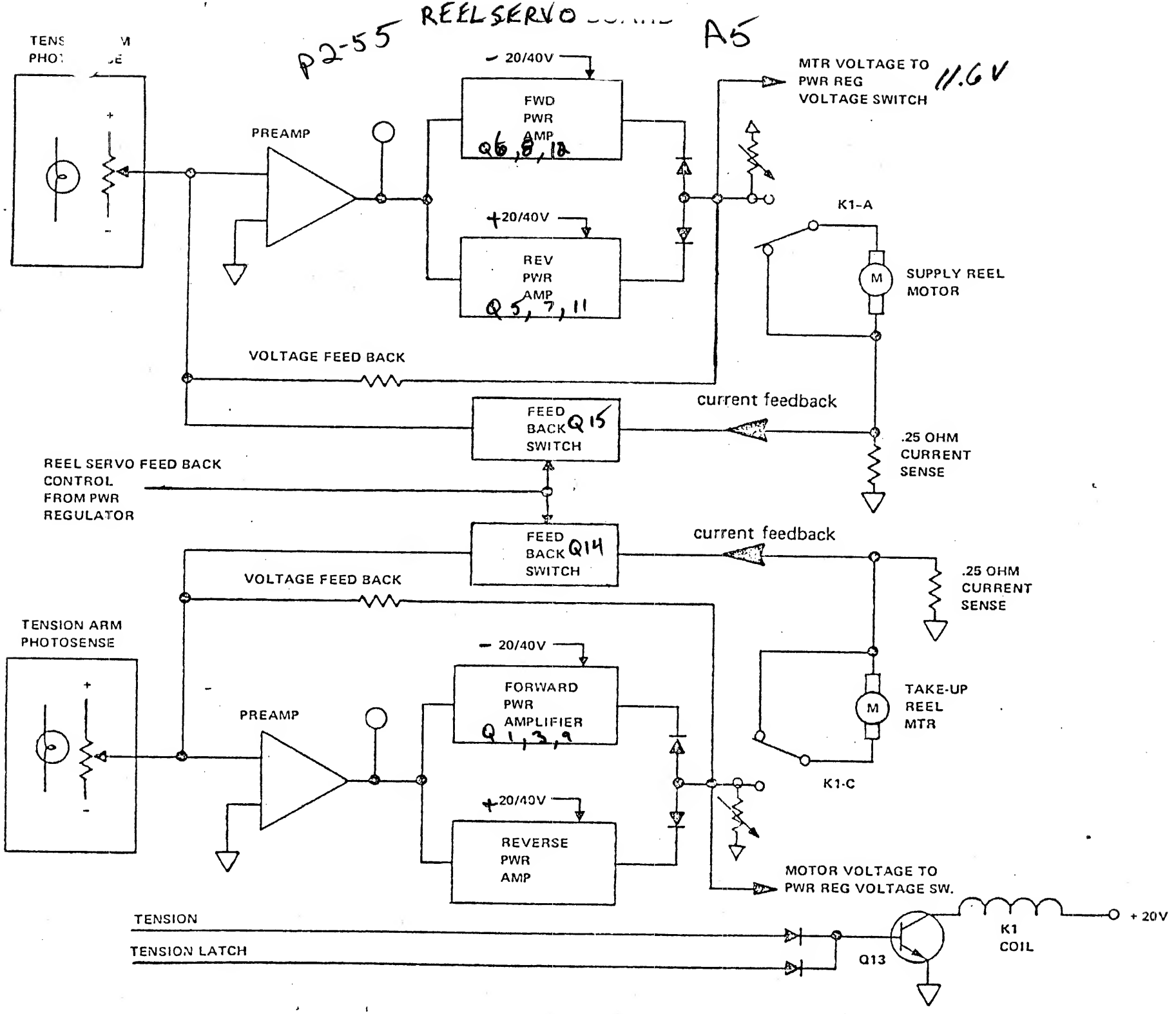
VI - A Reel Servo Block Diagram and Schematic

The reel servo board provides drive current for the reel motors relative to the tension arm position. Photosense assemblies on the tension arms provide input to the premplifier proportional to the amount and direction of tension arm movement. The preamp simulaneously feeds two complimentary power amplifiers. The appropriate power amplifier drives the reel motor causing the tension arm to return to its center position.

Synchronous tape speeds utilize voltage feedback which allows the tension arms more travel and decreases the motor duty cycle. However, when a high speed operation takes place in a tape unit, the reel servo feedback control line goes negative and current feedback is gated into use. This provides more restrictive feedback and causes the motors to react more per change in tension arm position, thus keeping the tension arm more nearly centered. Supply voltage to the power amplifier is controlled by the voltage switch on the power regulator. The motor voltage is fed to the voltage switch which senses an excess of approximately 11 volts indicating the tension arm is approaching its limits. When this voltage is reached and the unit is in a high speed operation, the appropriate polarity 40 volt supply is gated to the servo amplifier. This allows the reel motors sufficient voltage to maintain the high speed operation. R104 and 106 are used at synchronous tape speeds to compensate for the non-linearity of the tension arm deflection.

When power is initially turned on, the tension arms are against the limit switches disabling the 5V TAPE TENSION Signal. The LOAD pushbutton is in the N.C. position applying a ground to the bases of Q19 and Q13. With Q19 off, Q20 conducts applying OV on the TAPE TENSION signal. With Q19 off, Q18 is also off as well as Q16 and Q17. Therefore, Q16 and Q17 ground the inputs to the power amplifiers of the reel servo motors. With a ground at the base of Q13 through both diode CR11 and CR2 paths, Q13 is off and relay K1 remains deenergized keeping a short across both motors.

Depressing LOAD pushbutton turns on Q13 energizing K1 and Q19 which turns off Q20, Q16 and Q17. Relay K1 stays energized through R109 and CR11. The grounds are removed from the inputs to the power amplifiers since Q16 and Q17 are now off. The reel servo motor circuits are now enabled allowing the tape to be tensioned. As the tape is tensioned, tension limit switches


P2-55 REELSERVO A5
TENS PHOT
PREAMP
- 20/40V
FWD PWR AMP
Q6,8,10
+20/40V
REV PWR AMP
Q5,7,11
MTR VOLTAGE TO PWR REG VOLTAGE SWITCH
11.6V
K1-A
M
SUPPLY REEL MOTOR
VOLTAGE FEED BACK
FEED BACK SWITCH Q15
current feedback
.25 OHM CURRENT SENSE
REEL SERVO FEED BACK CONTROL FROM PWR REGULATOR
FEED BACK SWITCH Q14
current feedback
VOLTAGE FEED BACK
.25 OHM CURRENT SENSE
TENSION ARM PHOTOSENSE
- 20/40V
FORWARD PWR AMPLIFIER
Q1,3,9
PREAMP
M
TAKE-UP REEL MTR
K1-C
+20/40V
REVERSE PWR AMP
MOTOR VOLTAGE TO PWR REG VOLTAGE SW.
TENSION
TENSION LATCH
Q13
K1 COIL
+ 20V

close, enabling 5V to the base of Q19 through R46 keeping Q19 conducting. TAPE TENSION also maintains a constant forward bias on Q13 through CR11.

The voltage switching circuit (see power regulator) switches from ± 20V to ± 40V during a high-speed forward or reverse operation. These voltages supply the power for the reel servo power amplifiers.

The FEEDBACK CONTROL signal from the power regulator PCA supplies a + 8V or -8V signal to the FET switches Q15 and Q16.

When operating in a normal mode (synchronous or load speed), the servo operates with voltage feedback. The +8 volts from the feedback switching network (feedback control) back-biases the feedback FET switch. Feedback is then provided through R47 and R105. During a high-speed operation, the feedback control changes to -8 volts. The feedback FET switch is forward biased and the current feedback path is through the FET switch.

The reel servo tension arm assemblies contain dual element photo-conductors that are illuminated by a lamp shining through a slotted disc. The slot is in the form of a spiral attached to the tension arm. As the arm moves, the slot exposes different areas of the photo-conductor. As a result, the output of the photo-conductor is proportional to the position of the tension arm.

The reel servo preamplifer is an integrated operational amplifier that amplifies the position error of the tension arm. The tension arm photo-conductor output is single-ended, therefore, an off-set is provided by R39 or R41. The preamplifier drives a class B motor drive amplifier. The motor power amplifier has a gain of 10.

VI-C Capstan Servo Block Diagram and Schematic

The capstan servo consists of a capstan motor/tachometer and printed circuit assembly. The capstan is the only device on the 7970 transport used for driving tape. Therefore, the capstan drive servo amplifier must be capable of moving tape at 5 different speeds; forward/reverse synchronous, high-speed forward/reverse (160 IPS) and load point search speed (20 IPS). Capstan servo command lines enter the servo board from the control and status PCA and are applied to one of five reference voltage sources. Output from the high-speed forward and high-speed reverse voltage sources are adjustable and provide an input to a summing junction. Output from the forward and reverse synchronous sources is adjustable and provides input to the bi-polar ramp generator. The slope of the ramp generator output is adjustable to permit changing the start/stop distance; and provides synchronous speed input to the summing junction. The load point search voltage source provides a non-adjustable 20 IPS drive source to the summing junction.

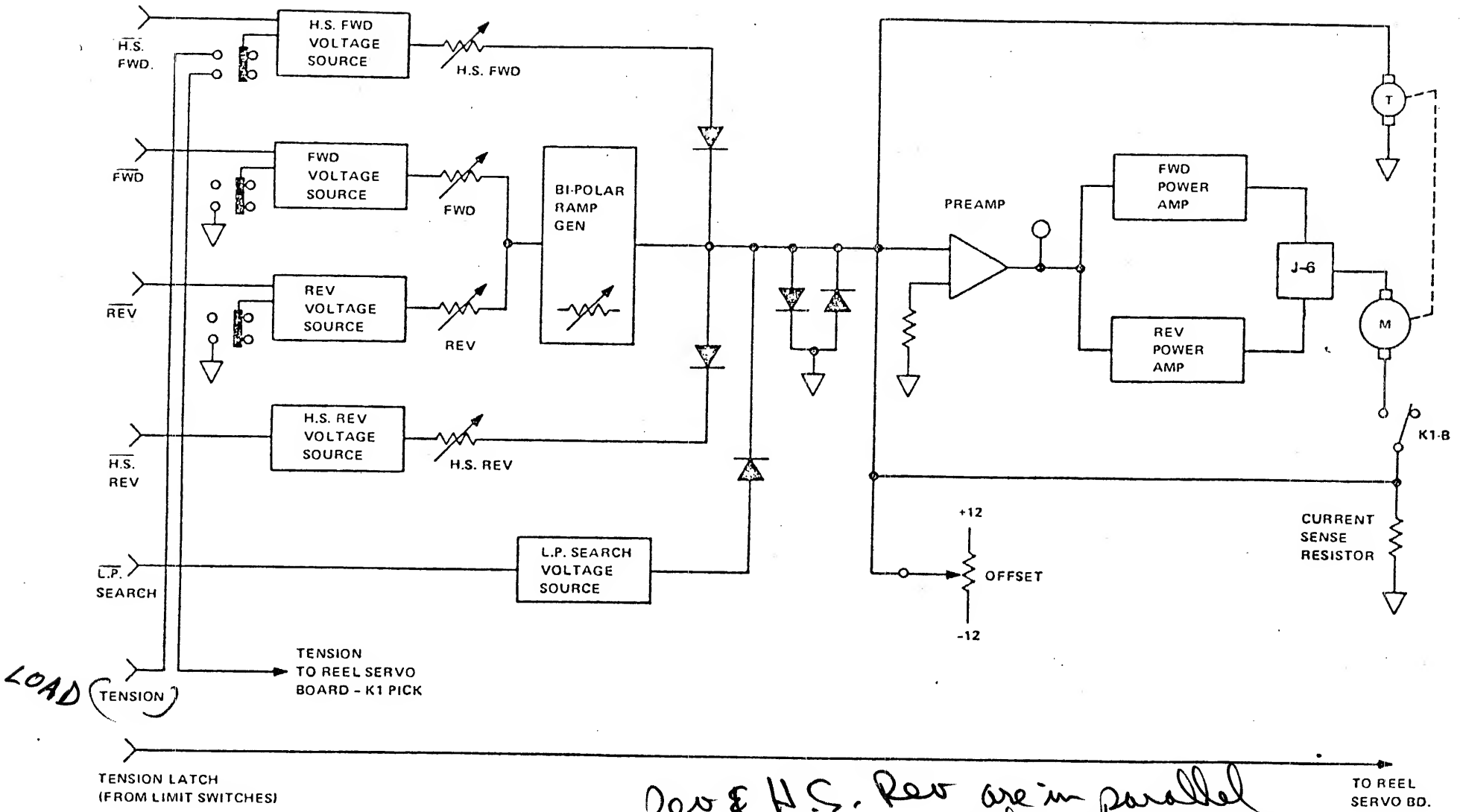
An offset potentionmeter is used to compensate for any component leakage and to "zero" the summing junction.

The summing junction provides input to a preamp which simultaneously feeds two complimentary power amplifiers. The appropriate power amplifier drives the capstan motor causing tape motion. Velocity feedback voltage relative to capstan speed is developed by a tachometer and is presented to the summing junction along with motor current feedback which is developed across the current sense resistor. These two feedback voltages oppose the applied drive voltage to maintain a uniform tape speed.

A connector (J-6) is placed in one of 6 positions to allow correct operation of the capstan servo motor assembly. Damage to the PCA or capstan motor may result if J-6 is missing or incorrectly installed.

The capstan motor is driven by current generated by integrating preamplifier U4 and motordrive amplifiers Q1 through Q6 on the capstan servo PCA. The direction and speed of the tape motion is controlled by the polarity and magnitude, respectively, of the current supplied to the motor by motor-drive amplifiers Q1 through Q6. Transistors Q2, Q4 and Q6 supply current for forward tape motion and Q1, Q3, and Q5 supply current for reverse tape motion.

CAPSTAN SERVO BOARD



Rev & H.S. Rev are in parallel which of course causes interaction

SAME FOR H.S. Foward & Foward

The polarity and magnitude of the current supplied to the capstan motor is determined by the polarity and magnitude of the algebraic sum of currents at the input (pin 2) to integrating preamplifier U4. This current-summing junction has four current sources; the bipolar ramp generator (U2, U3 and R66), the high-speed forward ramp circuit (U1B, Q8, C25, and Q9), the high-speed reverse ramp circuit (Q13, Q10, C26, and Q11), and the load point search voltage source (Q12). Clipping diodes CR17 and CR18 limit the input voltage to preamplifier U4 to a relatively low value.

The bipolar ramp generator consists of high-gain amplifier U2 and integrating amplifier U3. It converts the step voltage inputs from the forward and reverse voltage sources to positive-going (forward) and negative-going (reverse) ramp voltages. A clipping network (CR7 through CR11) limits the voltage at the point common to R39 and R40 to a maximum of approximately 7.5 volts, regardless of its polarity. Amplifier U2 is a saturating amplifier (with a voltage gain of approximately 100) with no phase inversion. Integrator U3 inverts its input, converting a positive step input to a negative-going ramp and a negative step input to a positive-going ramp. Negative feedback from the output of U3 to the input of U2 through R66, combines U2 and U3 into a single ramp generator. The feedback through R66 helps linearize the ramp voltage output supplied to the summing junction. The slope of the ramp is controled primarily by C28, R40, R41 and R43. Adjustment of the ramp slope is enabled by variable resistor R42.

With both the HSFWD and FWD signals inactive (high) and both the +160 and FWD switches in the off position, both inputs to U1D are high, Q7 is on, and zero volts is present at the junction of CR5, CR6, and R34. This leaves the voltage at the input to the bipolar ramp generator dependent on the input voltage supplied by the reverse voltage source.

When either the HSFWD or FWD signal is active (low) or one of the two switches is closed, Q7 is off. With Q7 off, a voltage of -6.2 volts is present at the junction of CR5, CR6, and R34. Assuming the output of the reverse voltage source (at the point common to CR1, CR2, and R28) is at zero volts, this applies a negative voltage to the bipolar ramp generator. This results in forward tape motion at synchronous speed. Variable resistor R34 adjusts the ramp generator input voltage to produce the desired forward synchronous tape speed.

With both the HSREV and REV signals inactive (low and high, respectively) and the REV switch in the open position, U1C applies zero volts to the point common to CR1, CR2, and R28. In this condition the voltage at the input to the bipolar ramp generator is dependent on the voltage supplied by the forward voltage source. If both the forward and reverse voltage sources supply zero volt outputs, the input voltage to the bipolar ramp generator will be zero volts and no tape motion will result.

If either the HSREV or REV signal is active (high and low, respectively) or the REV switch is closed, +6.2 volts will be present at the point common to CR1, CR2, and R28. With +6.2 volts present at the junction of CR1, CR2, and R28, a positive voltage is supplied to the bipolar ramp generator input. This results in reverse tape motion at synchronous speed. Variable resistor R28 is used to adjust reverse synchronous tape speed by adjusting the input voltage to the bipolar ramp generator.

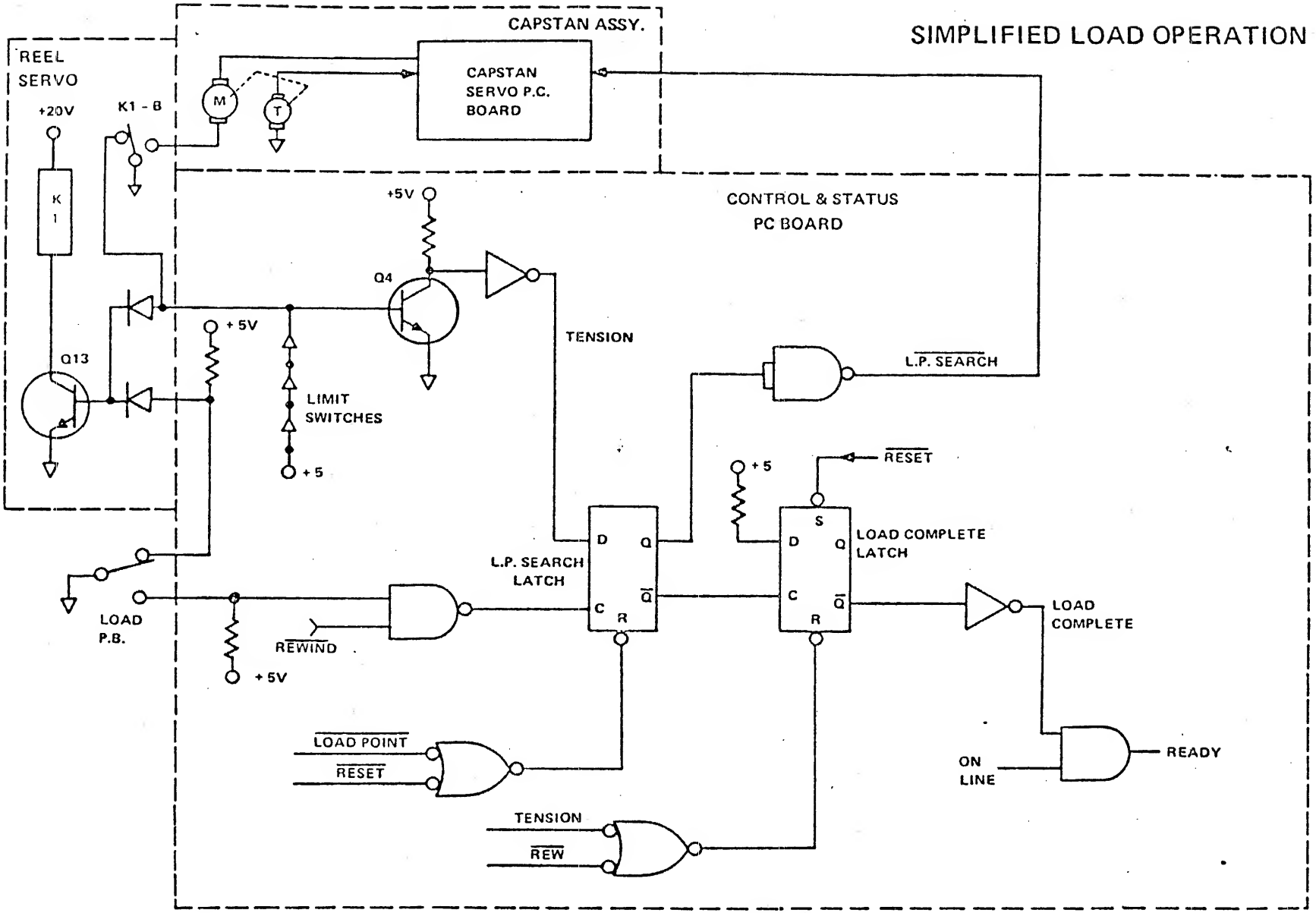
When the HSFWD signal is inactive (high) and the +160 switch is in the open position, the output of U1B is zero volts, Q8 is on, C25 has little or no charge, and Q9 is off, supplying zero volts output to the summing junction through R52 and R53. When the HSFWD signal becomes active (low) or the +160 switch is closed, Q8 is cut off and C25 starts to charge toward a voltage somewhere near +3 volts (depending on the setting of variable resistor R53). This draws current through the base-emitter diode of Q9. This current increases as the charge on C25 increases, supplying a positive-going ramp voltage to the summing junction. At the same time, the bipolar ramp generator is supplying a second positive-going ramp voltage to the summing junction because the forward voltage source is activated whenever the high-speed forward ramp circuit is activated. Currents from these two ramp voltages are summed at the summing junction to produce a forward tape speed of greater magnitude than the synchronous speed. The high-speed forward tape speed is adjusted to 160 inches per second by adjusting R53.

Operation of the high speed reverse ramp circuit is similar to that of the high speed forward ramp circuit except that the active level of the HSREV signal is the high level and the ramp voltages supplied to the summing junction by the high speed reverse ramp circuit and the bipolar ramp generator are negative-going ramps.

When the Load Point Search signal is inactive (high), Q12 is on and zero volts is applied to the summing junction. When the Load Point Search signal is active (low), Q12 is off and a positive voltage, sufficient to produce a forward tape speed of approximately 20 inches per second, is applied to the summing junction through R61 and R63.

A notch filter in the velocity feedback circuit from the tachometer is selected to attenuate the mechanical response of the motor-tachometer combination. A compensating network in the current feedback circuit is also selected, depending upon synchronous speed of the tape unit. When power is removed or tape tension is lost, the return from the capstan motor to the current sense resistor is opened by a relay located on the reel servo printed-circuit assembly.

SIMPLIFIED LOAD OPERATION



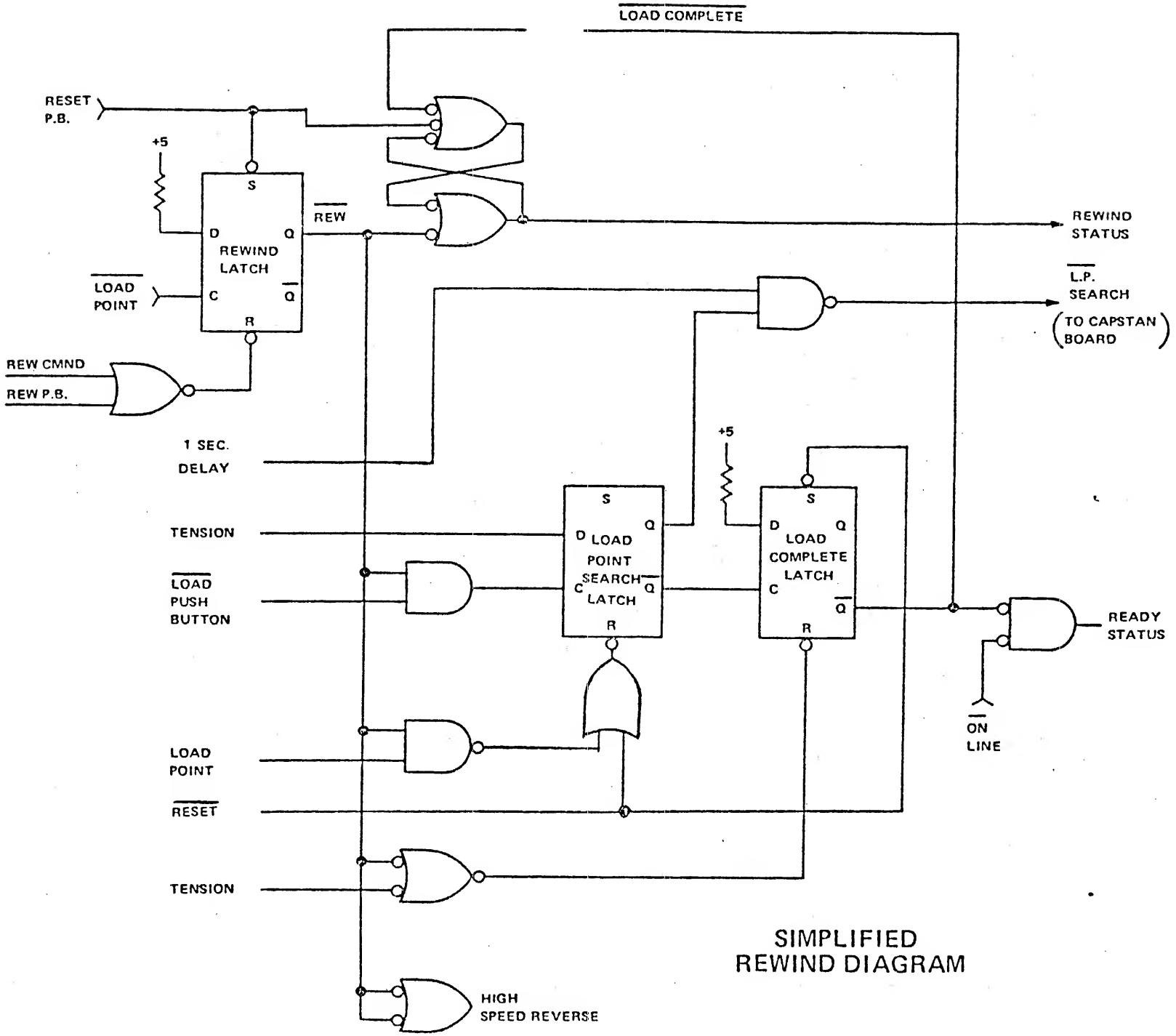
VI-E Simplified Load Operation

The diagram representing a load operation includes portions of the reel servo, capstan servo, and the control and status PC assemblies. Pressing the load pushbutton initiates a load operation by turning on Q13 which energizes relay K1 on the reel servo board. Energizing K1 transfers control of the capstan and reel motors to their respective servo amplifiers. Since, at this time the tension arms are at rest, the supply reel drives reverse and the take-up reel drives forward pulling the tension arms to their center poistion. This allows the tension arm limit switches to close and provide a holding path for relay drive transistor Q13. Transferring the limit switches also allows transistor Q4 to turn on which provides a "tension" indication to the L.P. search latch. Releasing the load pushbutton "clocks" the L/P. search latch to the set condition, initiating a L.P. search command for the capstan servo. Reaching the L.P. reflector tab or pressing the reset pushbutton generates a direct reset for the L.P. latch dropping the L. P. search command and clocking the load complete latch to the set state. This generates a load complete signal which is "anded" with ON LINE and sent to the interface as READY status. A second method of generating READY status is providing a rest signal to the direct set input of the load complete latch while tension is true. This directly sets the load complete latch. If the H/S FORWARD switch on the capstan servo PCA is placed in the true position K-1 will not energize. Hence the tape will not load.

VI-G Simplified Rewind Operation

A rewind operation is initiated by a REWIND command from the interface or by pressing the REWIND pushbutton. Both methods provide a direct reset to the rewind latch which generates a $\overline{\text{REW}}$ signal. The $\overline{\text{REW}}$ signal initiates high speed reverse, sends rewind status to the interface, and resets the load complete latch which drops ready status.

With the tape unit rewinding (HS reverse), passing the load point clocks the rewind latch and negates $\overline{\text{REW}}$ command. Dropping the $\overline{\text{REW}}$ command, negates rewind status and clocks the L.P. search latch. Setting the L.P. search latch gates a load point search command to the capstan board if "delay" from the power regulator is positive. This delay is to insure that the rewind command is completely negated prior to starting the L.P. search. Completing the L.P. search (reaching the L.P. tab or pressing reset) sets the load complete latch which gates ready status to the interface.



SIMPLIFIED
REWIND DIAGRAM

VII-A NRZI Write Electronics

The Write electronics is primarily contained on the Write Control and dual or single channel write data PCAs.

$\overline{WSW}$ and $\overline{FWD}$ signals are activated for approximately 20MS at the same time. $\overline{WSW}$ establishes the S-R inputs for the Write latch. $\overline{FWD}$ is delayed by the forward integrator to allow the write command to settle, and then clocks the write latch. The Q and $\overline{Q}$ outputs of the write latch enables CLAMP and WRITE PERMIT to all write data channels. CLAMP arrives at the write toggle FF slightly behind WRITE PERMIT because of an additional gate delay.

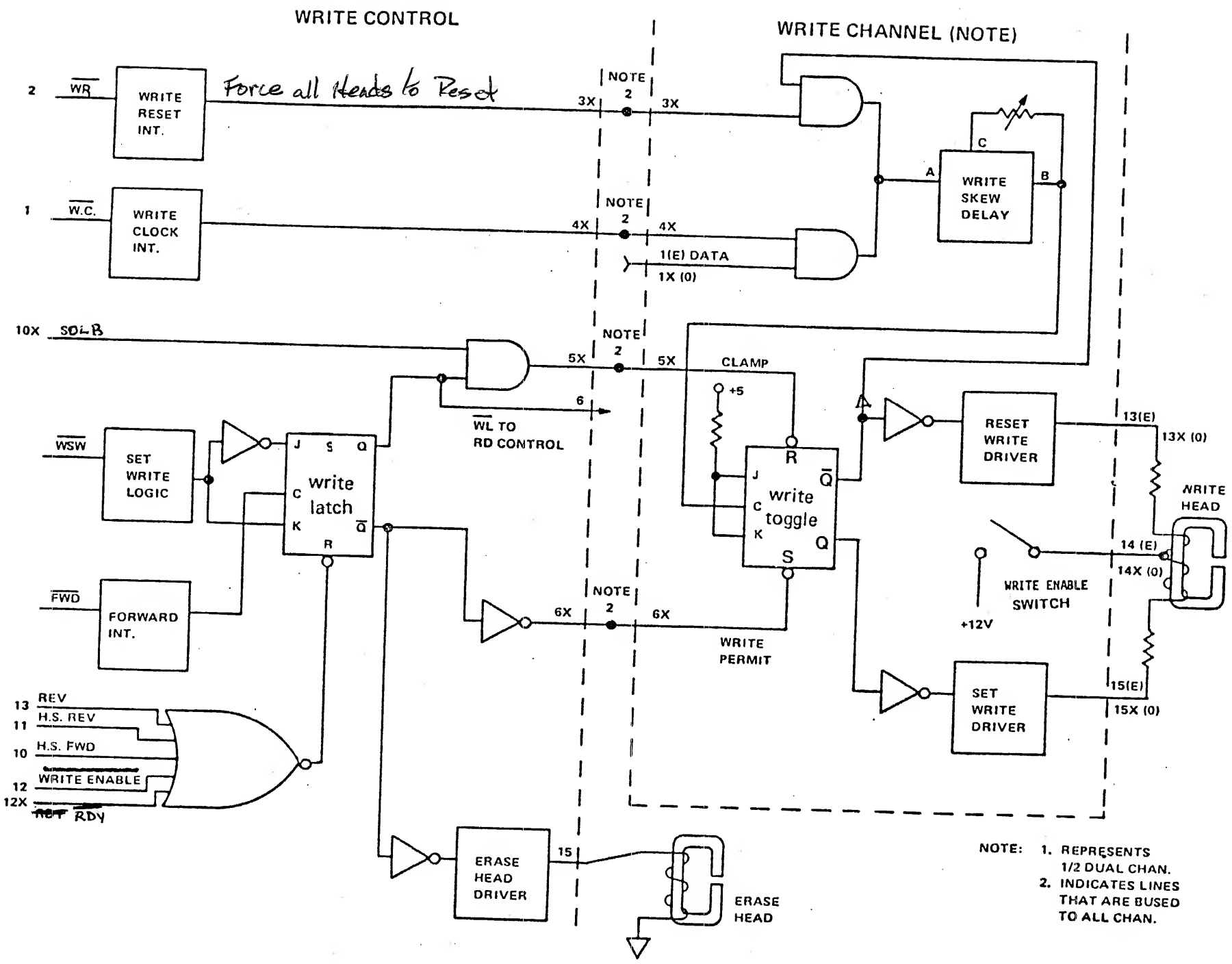
The write toggle FF is on the write data PCA. Initially, CLAMP and WRITE PERMIT are both false causing both the Q and $\overline{Q}$ outputs of the write toggle FF to be true, degating both Write drivers. Since CLAMP is delayed slightly with respect to WRITE PERMIT, the write toggle FF is forced into the reset state. Transistor Q1 turns on enabling current to flow through the write reset head resetting flux at the tape.

Write clocks ($\overline{WC}$) from the interface enter the write clock integrator which delays the clock to allow the data to settle before clocking the write skew delay one-shot. The output of the write clock integrator is "anded" with data in each channel and sent to the write skew delay one-shot. The one-shot is triggered by the "anded" output of data and write clock delayed. The one-shot output triggers the write toggle FF. Each one-shot pulse changes the state of the write toggle FF which alternately causes the reset and set drivers to conduct. After all data characters have been written, WRITE RESET (WRS) is sent from the interface to the write control PCA. WRS is "anded" with the Q output of the write toggle FF which generates one more flux reversal if an odd number of bits was written in the channel. All write toggles are therefore left in the reset state. The LRC character is written on tape as a result of returning all write toggle flip-flops to the reset state.

The center tap on the write head received +12 volts. The +12V is enabled by the write enable solenoid whenever a tape is mounted equipped with a write enable ring.

The $\overline{Q}$ output of the write latch turns on Q4 enabling the drive current in the erase head and $\overline{\text{WRITE STATUS}}$ to the interface. The Q output of the Write latch enables $\overline{\text{WRITE LATCH}}$ to the read electronics.

The skew delay one-shot allows delaying data in the channel in which it is located so that the data bits will be written at the same time as the data bits in the channel with the greatest lag time due to skew. The skew adjustment (R11) on the one-shot provides the adjustment required to align each channel so that the data bits for all channels will be written at the required time to correct for write head static skew.


WRITE CONTROL
WRITE CHANNEL (NOTE)
2
WR
WRITE RESET INT.
Force all Heads to Reset
NOTE 2
3X
3X
1
W.C.
WRITE CLOCK INT.
4X
4X
1(E) DATA
1X (0)
C
A
B
WRITE SKEW DELAY
10X SOLB
5X
5X
CLAMP
+5
6
WL TO RD CONTROL
WSW
SET WRITE LOGIC
J S Q
C write latch K Q
R
FWD
FORWARD INT.
6X
6X
WRITE PERMIT
R
J Q
C write toggle K
S
RESET WRITE DRIVER
13(E)
13X (0)
WRITE HEAD
14 (E)
14X (0)
WRITE ENABLE SWITCH
+12V
SET WRITE DRIVER
15(E)
15X (0)
13 REV
11 H.S. REV
10 H.S. FWD
12 WRITE ENABLE
12X NOT RDY
ERASE HEAD DRIVER
15
ERASE HEAD
NOTE: 1. REPRESENTS 1/2 DUAL CHAN.
2. INDICATES LINES THAT ARE BUSED TO ALL CHAN.

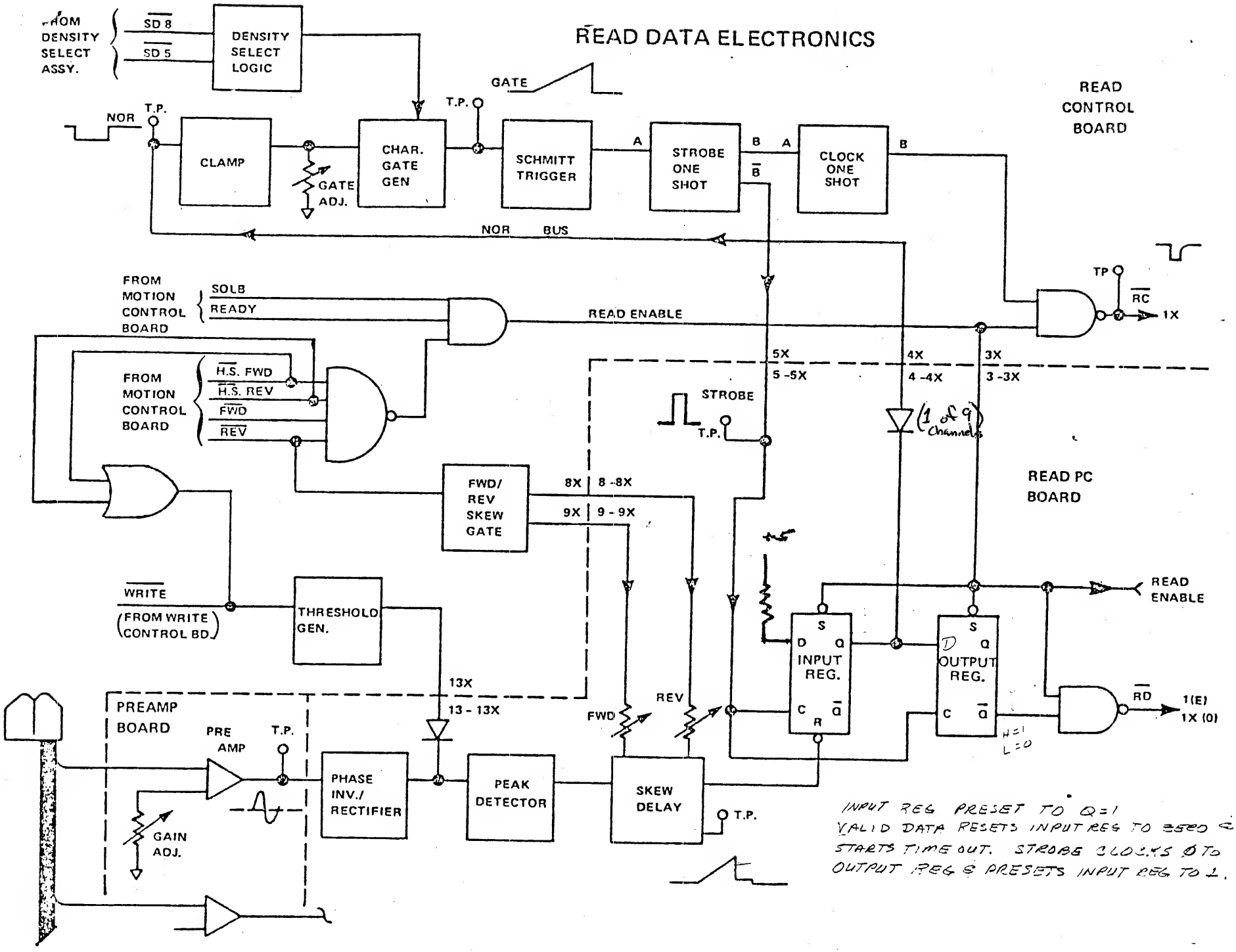
VII-B NRZI Read Electronics

The function of the read electronics is to receive an analog signal from the head assembly and convert it to a digital output. The associated read electronics block diagram represents the read preamp, the read control, and one channel of a dual-channel read PC board.

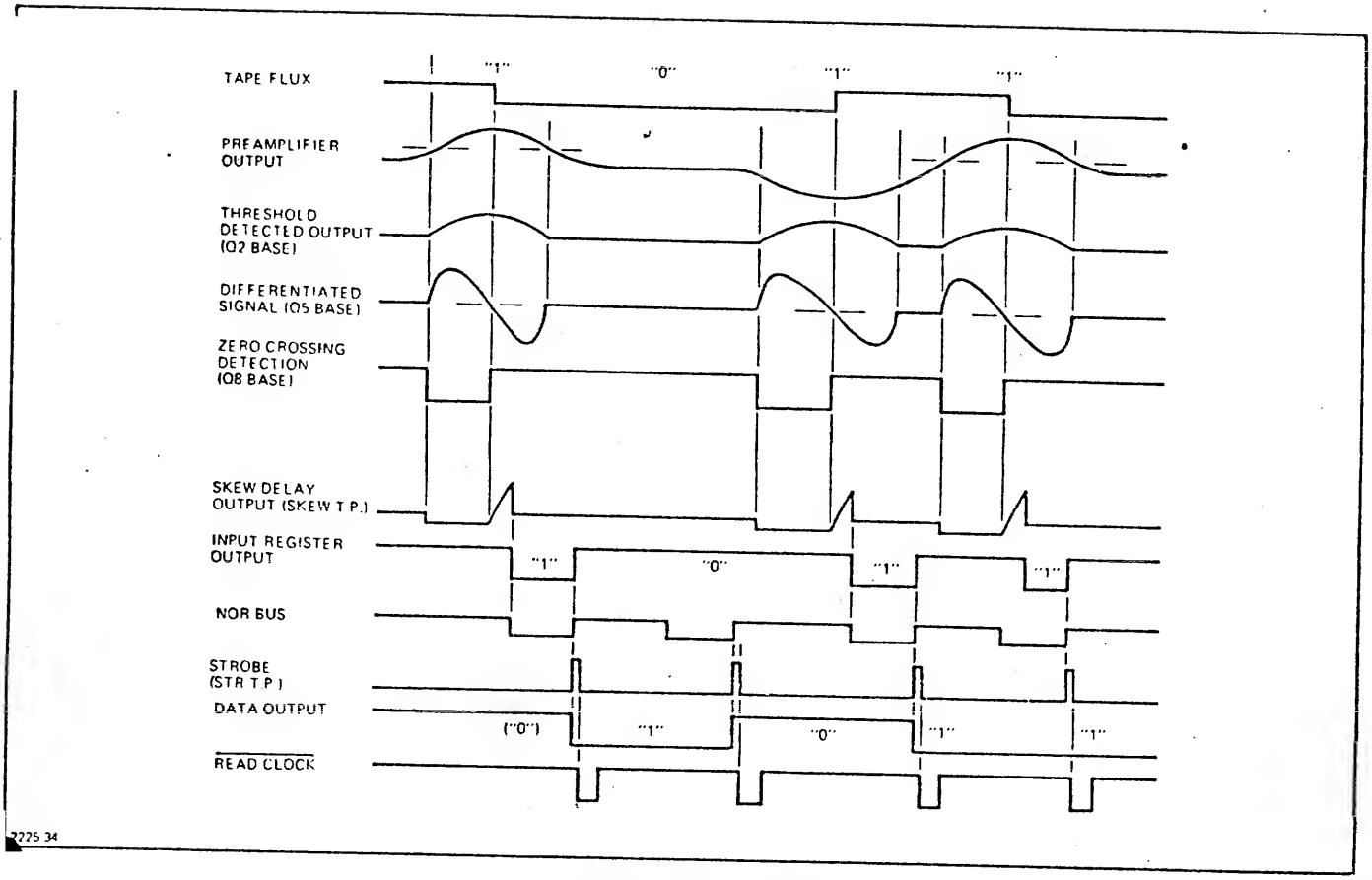
Tape moves across the read head inducing flux changes in the read head which become analog signals. These analog signals are preamplified by an adjustable single stage operational amplifier. The operational amplifier output signal is inverted and detected on the read data PCA (the zero crossover point is much more precisely detected than the sine wave peak). A threshold voltage generated on the read control PCA guards against noise triggering. The threshold input to the read data PCA establishes bias for this threshold detector diode covering approximately 40% base line clipping during write operations and 20% clipping during read operations. This clipping is accomplished to eliminate write to read crosstalk during write operations and provide noise immunity during read operations. The purpose of the peak detector is to represent the peak of the input signal with a sharp positive going edge of a square wave. This edge triggers the skew delay circuit which is used to compensate for static skew. Forward and reverse adjustments are provided for compensating for skew in both directions. When the skew delay ramp times out, a short duration negative going pulse directly resets the input register. Resetting the input register puts a "low" on the NOR bus (All nine channels are "wire-ored" to the NOR bus).

This "low" triggers the clamp circuit in the read control board, which in turn, starts the character gate time-out. The character gate ramp is coupled to the strobe one-shot through a Schmitt trigger. At the fall of the adjustable character gate ramp, the strobe one shot is fired, which sends a strobe pulse to the input and output registers as a clock. This strobe clocks the input register to its initial set condition and clocks the output register set for a logic zero and reset for a logic one. The trailing edge of the strobe triggers the clock one shot. This output is "anded" with READ ENABLE and presented to the interface as READ CLOCK. The READ ENABLE signal is used to enable the read clock, input register, output register, and output gate.

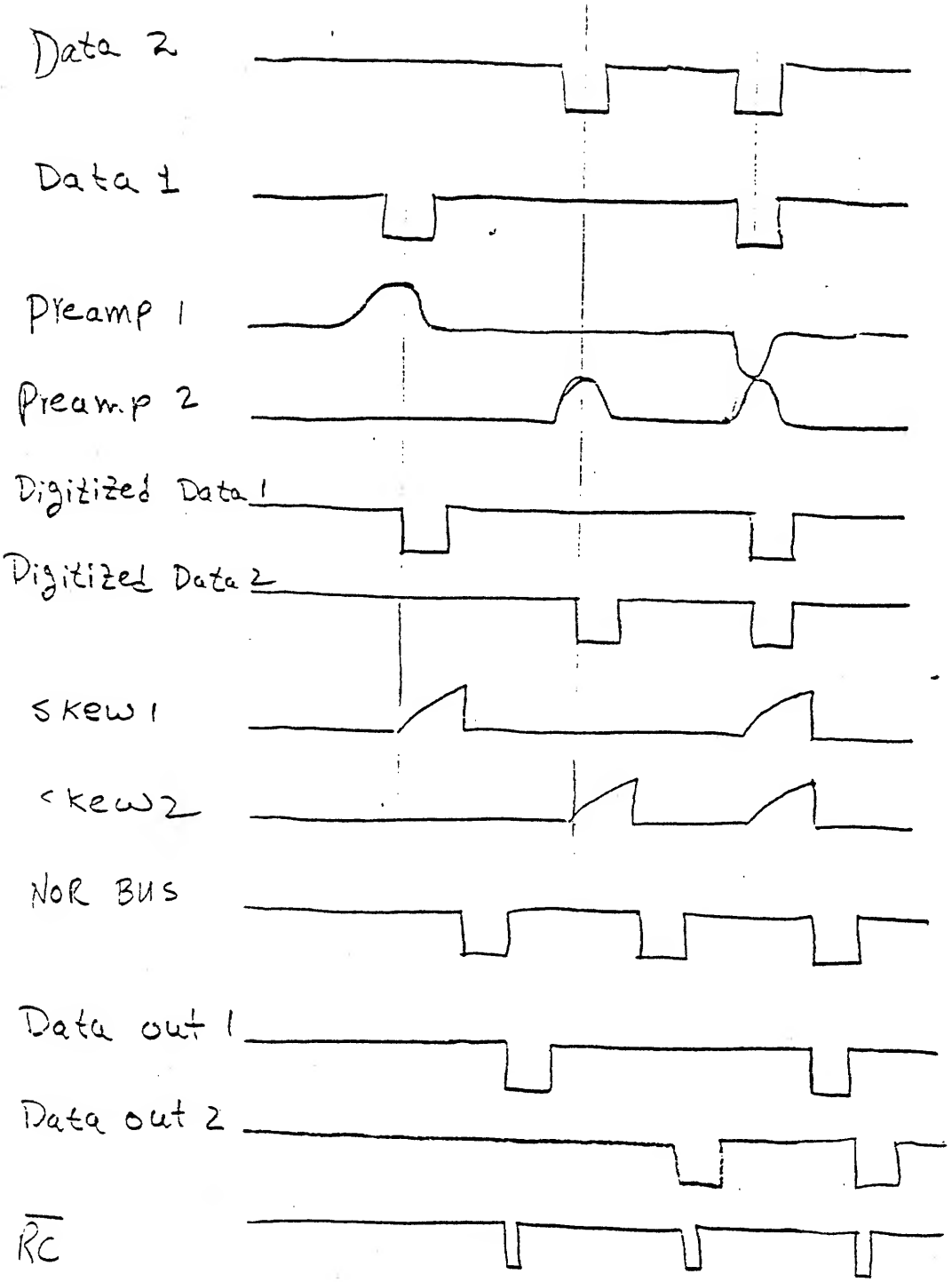
READ DATA ELECTRONICS



INPUT REG PRESET TO Q=1
VALID DATA RESETS INPUT REG TO ZERO & STARTS TIME OUT. STROBE CLOCKS Ø TO OUTPUT REG & PRESETS INPUT REG TO 1.



NRZI Circuits Waveforms



NRZI Circuits Waveforms
(two data channels)

During high speed read operation the threshold bias level is changed to maintain approximately 40% baseline clipping for proper noise immunity.

If a "0" occurs at the input of the read data PCA, the full wave rectifier, buffer, peak detector, high-gain amplifier, skew delay RC circuit, threshold generator, and input register will remain inactive. Since the input register has not stored a "1" when the Read Strobe occurs, a "0" will be stored in the output register and clocked out to the interface. The read control circuits operate as previously described to produce the Read Strobe because a"1" must occur on at least one of the nine channels for every byte. If no data bits occur, parity is set.

The first of nine data channels to arrive at the NOR bus triggers it. The other bits of a given character will appear within the NOR bus window after it has been triggered. The character gate determines the NOR bus window time. The window is adjusted to 46% of the bit spacing time. The adjustment is accomplished by varying R29 on the read control PCA.

VIII. PE Tape Drives

A. PE Recording

In NRZI recording, a change in flux was required to write a "one" while no change in flux was required to write a "zero".

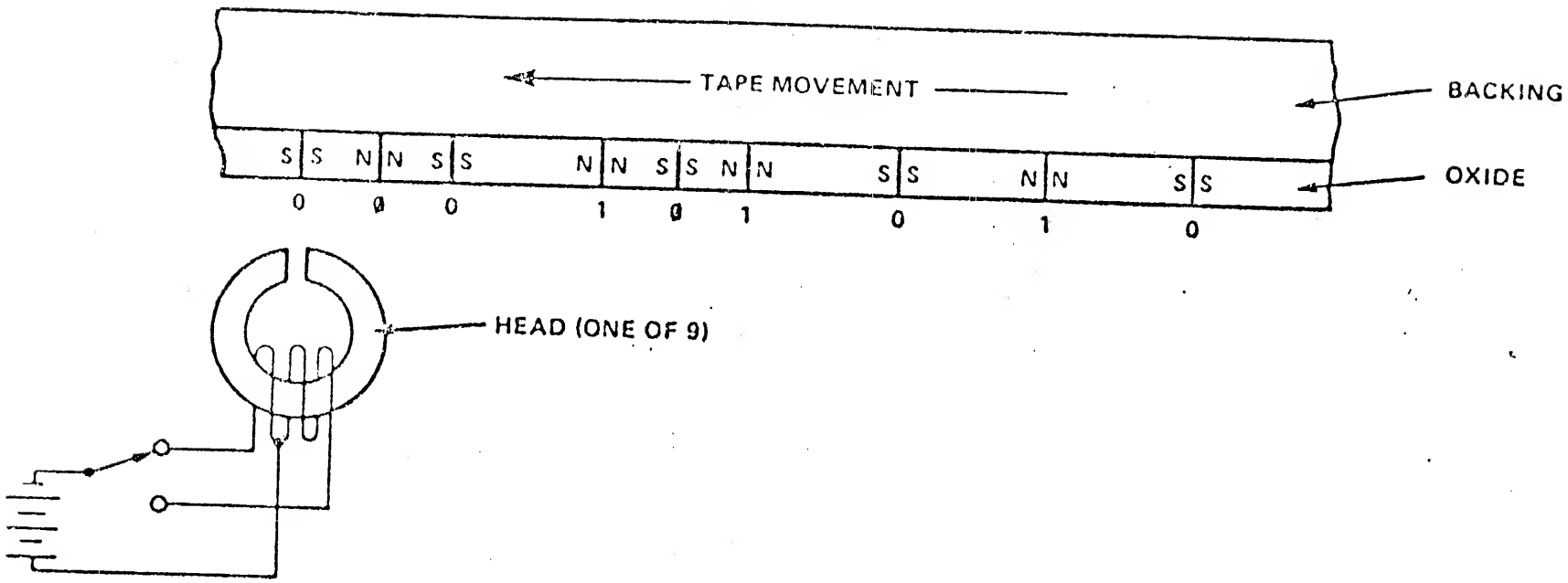
To accomplish phase encoded recording, a change of flux is required to write a "one" or a "zero". A change of flux in one given direction writes a "one" and a change of flux in the other direction writes a "zero". Since the polarity (phase) of flux determines whether we write a "one" or a "zero", a correction (phase correction) must be inserted between like data bits to establish the correct reference state (set or reset) for the next bit to be written. By monitoring the present state and the next bit to be written, the interface or optional write data formatter will determine if a phase correction is required. The drive write electronics contains no look ahead electronics.

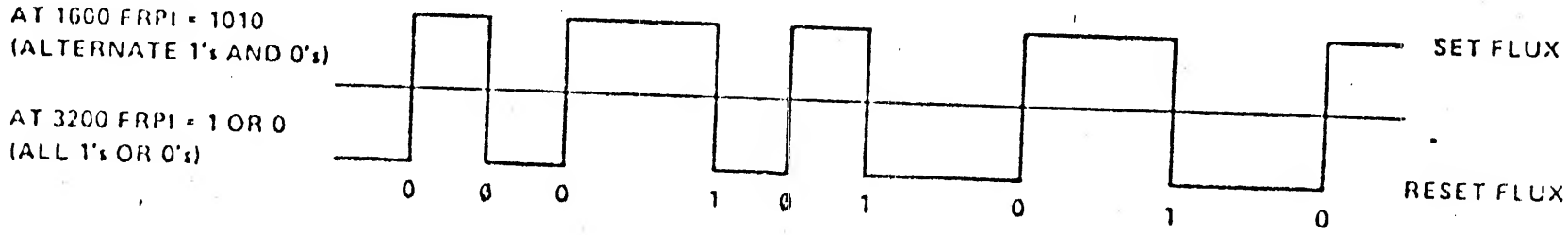
The write head is similar to the primary windings of a transformer with a center tap. By providing current to one side (set) or the other side (reset) the magnetic polarity of poles will change at the gap.

A change in flux on the tape from set to reset is either a logic "one" or a phase correction. A change from reset to set is either a logic "zero" or a phase correction. A phase correction occurs only between consecutive "ones" or "zeros". Phase corrections are both set and reset transitions. Their purpose is simply to occur as needed to place the tape in the current flux state so that the next logic "one" or "zero" can be written.

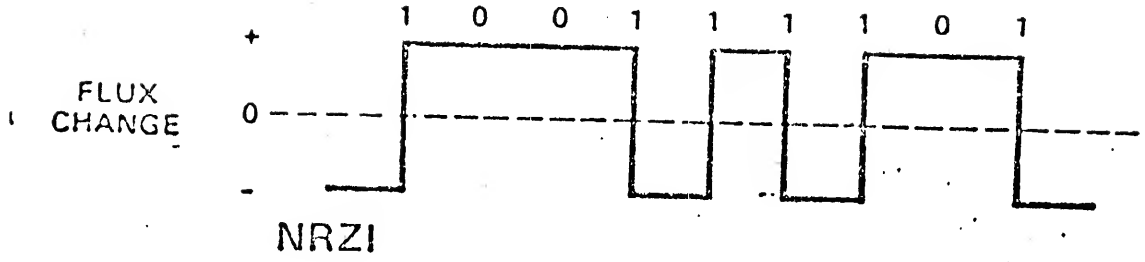
From the previous, it becomes apparent that there are only two possible rates of change of flux in PE recording. These rates are 1600 FRPI and 3200 FRPI.

PE RECORDING

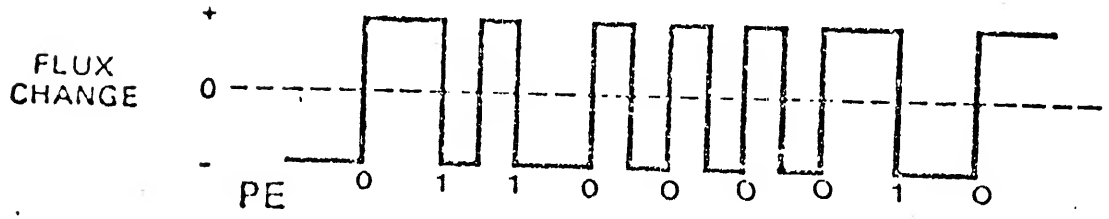




NRZI VERSUS PE



FLUX-TRANSITION ONLY FOR "1" BIT



FLUX TRANSITION FOR EACH BIT MAKES DATA REDUNDANT AND SELF CLOCKING

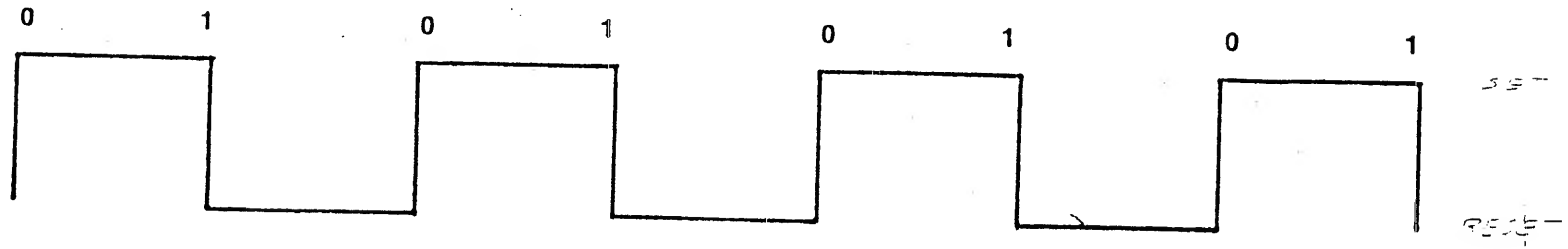
REDUCES PULSE CROWDING

PE 1600 VS 3200 FRPI

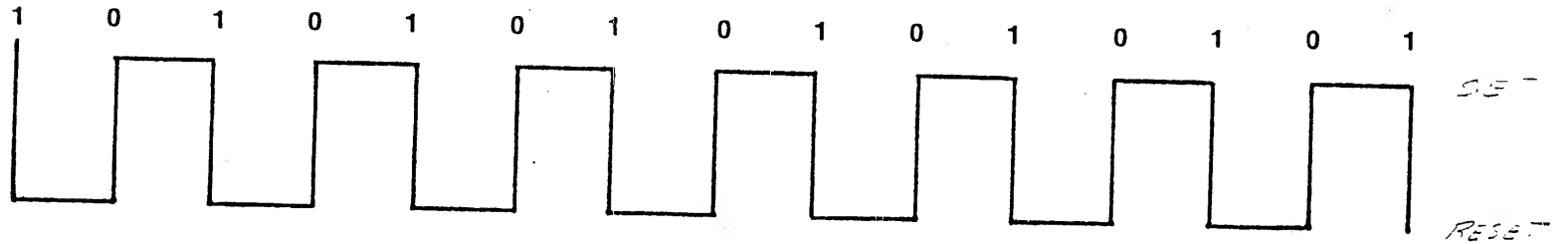
0=Phase Transition
0="0" Bit
1="1" Bit

FRPI=Flux Reversals Per Inch

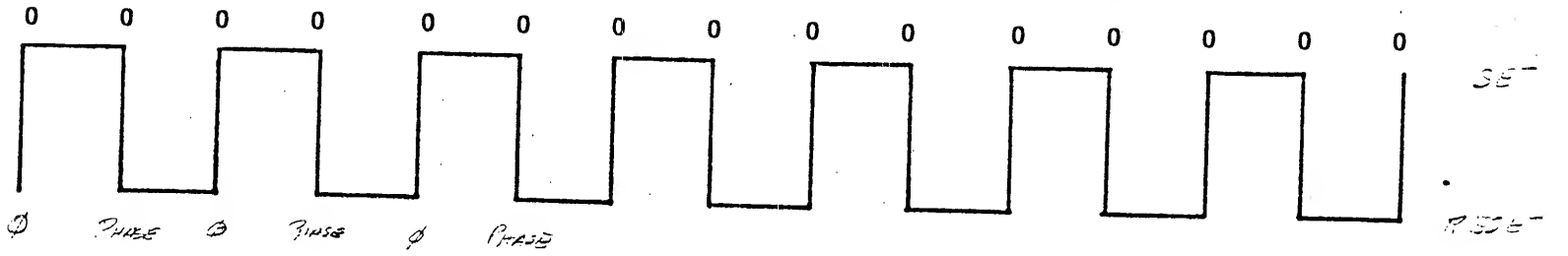
ALTERNATING "1"s AND "0"s = 1600 FRPI



ALL "1"s = 3200 FRPI



ALL "0"s = 3200 FRPI



VIII-C PE Format

PE tape information consists of three types of information blocks; identification burst blocks, data blocks, and tape (file) mark blocks. The identification burst (IDB) consists of flux reversals in the parity channel only. It begins slightly ahead of the beginning of tape (BOT) marker and ends slightly after the BOT marker. The first data block follows the IDB after a gap of a least 3 inches. A data block consists of three parts of sections; a preamble, data section, and a postamble. The preamble consists of 41 bytes; 40 logic "0" bits in every channel followed by one logic 1 bit in every channel. The data section normally consists of 18 to 2048 bytes. However, it can be of any desired length. The postamble is a 41 byte section which consists of one logic 1 in every channel followed by 40 logic 0's. Data blocks are separated by inter-block gaps greater than 0.5 inch long. Tape marks are used to separate data blocks into groups or files. A tape mark consists of from 64 to 256 flux reversals in channels two, six, and seven. (IBM channel numbers), or channels P, zero, and five. However, at the same time channels one, three, and four (IBM) must be without flux reversals.

Tape formats for NRZI and PE recording are similar. The PE tape format requires eighty-two bytes for the preamble and postamble.

The space between adjacent flux transitions determines the density. PE drives record at 1600 characters per inch (CPI) while NRZI recording is limited to 800 CPI.

FLUX REVERSALS ↑ = 0 (SET) ↓ = 1 (Reset)
(PHASE CORRECTION)

PREAMPLE = 41 CHARACTERS
40 Zeros in all channels
1 one in all channels

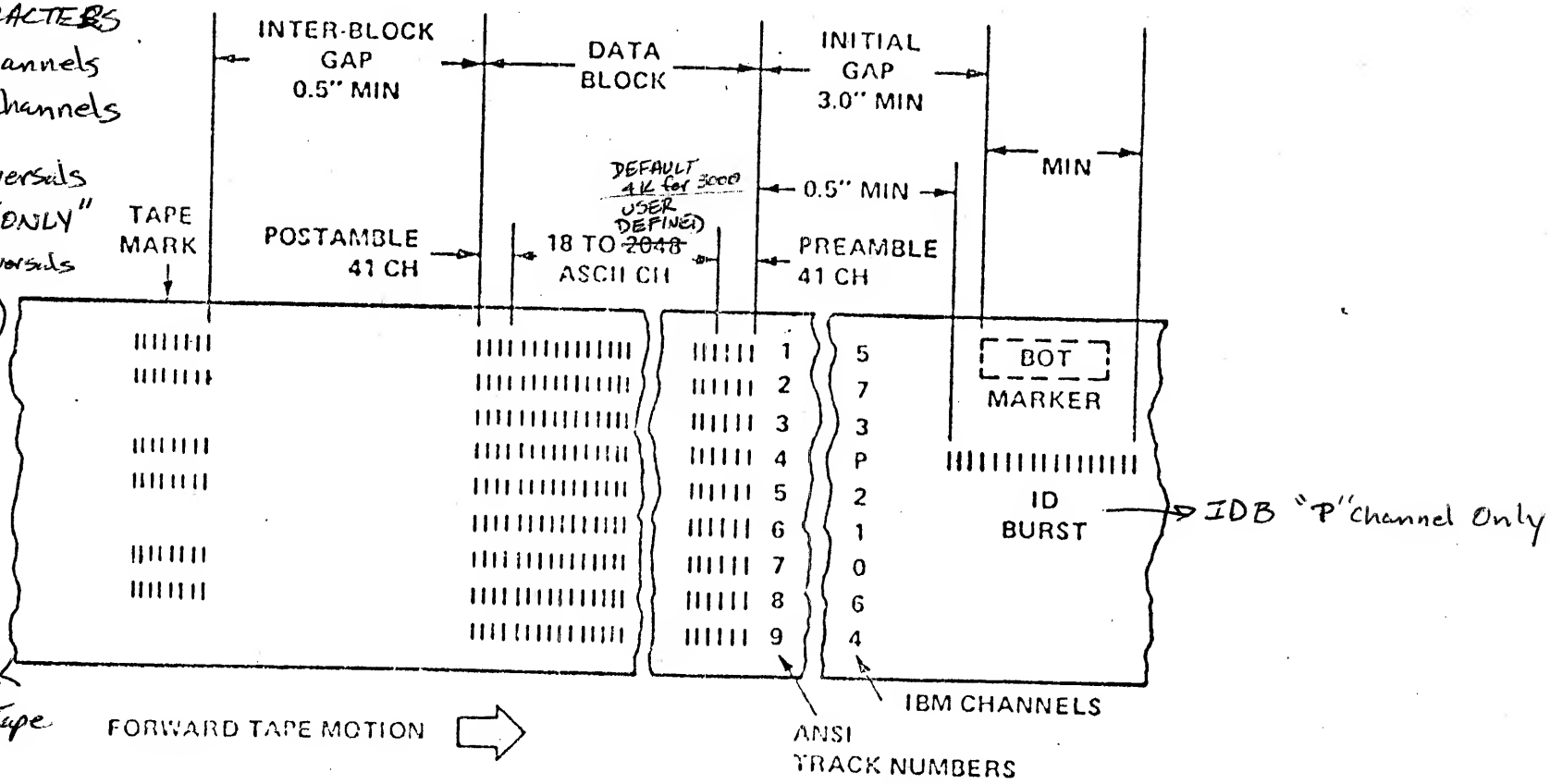
POSTAMPLE = 41 CHARACTERS
1 one in all channels
40 Zeros in all channels

TAPE MARK = Flux Reversals
Channels 2, 6, 7 "ONLY"
Approx. 64 to 256 Flux Reversals
(6 channel Tape Mark is an option. P, 8, 5)

ID BURST
P-channel "Only"

DOUBLE TAPE MARK
End of Data on Tape

NINE TRACK 1600 CPI PHASE ENCODED FORMAT



- TAPE MARK CONSISTS OF FROM 64 – 256 FLUX REVERSALS IN TRACKS 2, 5, 8
- ADDITIONAL REVERSALS IN TRACKS 1, 4, 7 (USER OPTION)
- TRACK WIDTH AND SPACING AS IN 800 CPI NRZI

NINE TRACK FORMAT COMPARISON

	800 CPI NRZI	1600 CPI PE
IDENTIFICATION BURST	NO	YES
PREAMBLE	NO	YES
MINIMUM BLOCK LENGTH	18 CHARACTERS	18 CHARACTERS
POSTAMBLE	NO	YES
CRCC	YES	NO
LRCC	YES	NO
TAPE MARK	YES	YES

IX. PE Read/Write Electronics

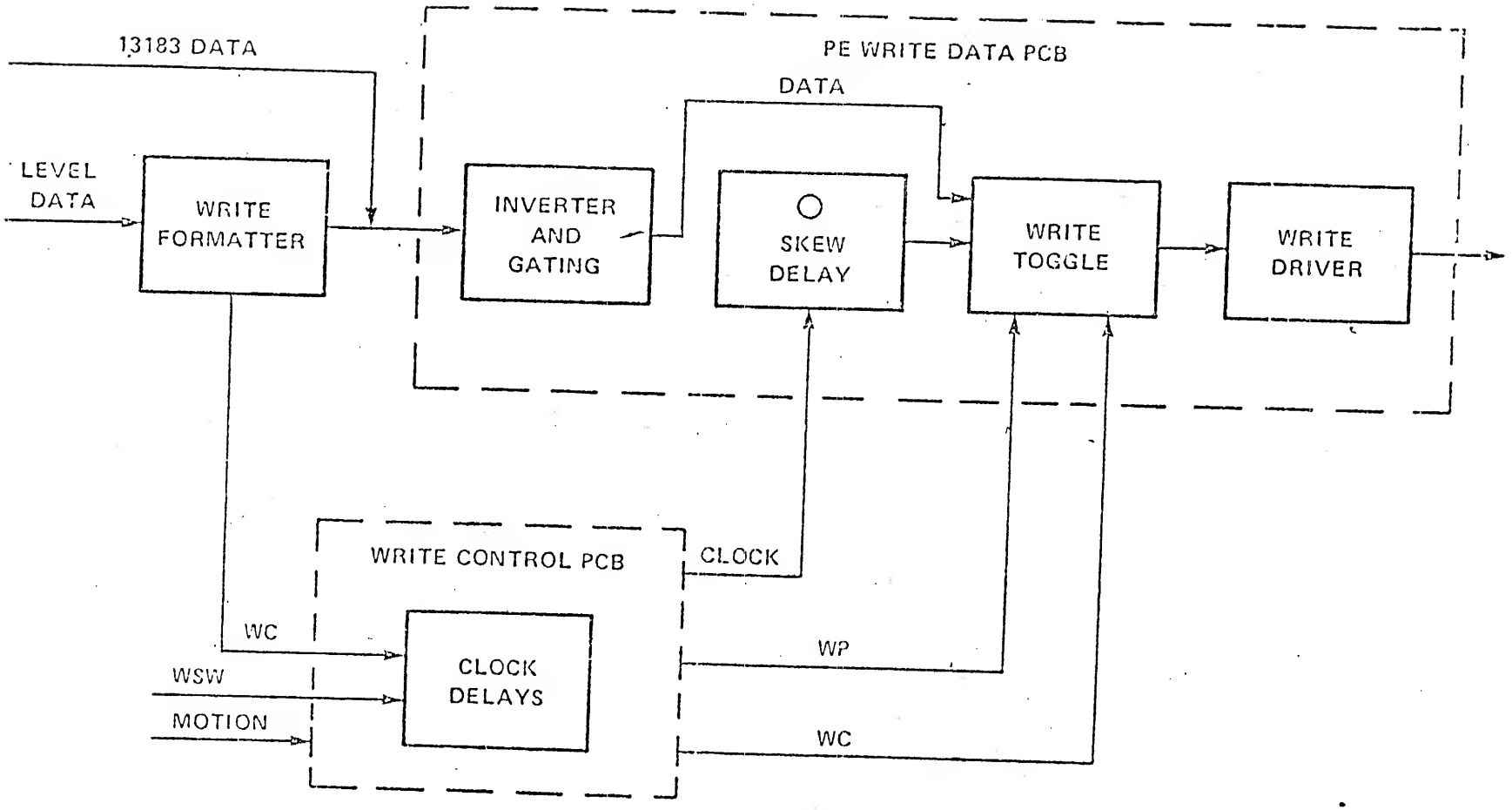
A. Write Electronics

The write electronics are similar for NRZI and PE recorders. Both PE and NRZI use the same write control PCA. The write reset circuitry is not required for the PE drive.

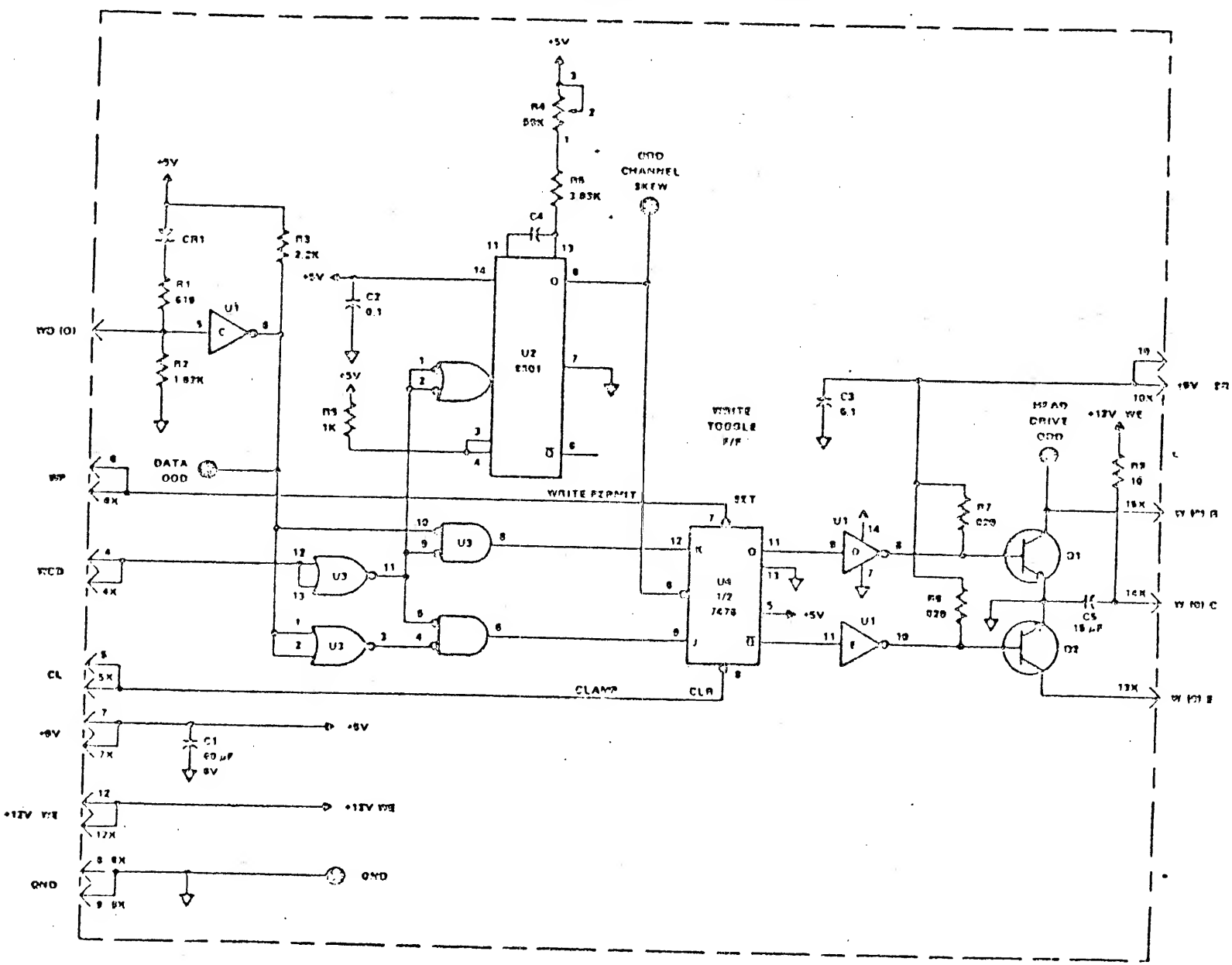
The write data PCA is similar for PE and NRZI. The write clock frequency from the interface is at twice the data frequency of that for NRZI. The function of the write toggle FF and write skew delay one-shot is the same for PE as previously described for NRZI. The circuitry ensures that current intially flows through the reset winding when a write command is received.

Variable resistor R4 controls the write skew delay. If R4 is set such that the entire 50K resistance is in the circuit, each succeeding clock will retrigger the one-shot before it has timed out. Thus, there will be no flux transitions recorded on tape.

PE WRITE


13183 DATA
PE WRITE DATA PCB
DATA
LEVEL DATA
WRITE FORMATTER
INVERTER AND GATING
SKEW DELAY
WRITE TOGGLE
WRITE DRIVER
WRITE CONTROL PCB
CLOCK
WC
WP
WSW
CLOCK DELAYS
MOTION
WC

SINGLE CHANNEL PE WRITE DATA PCA



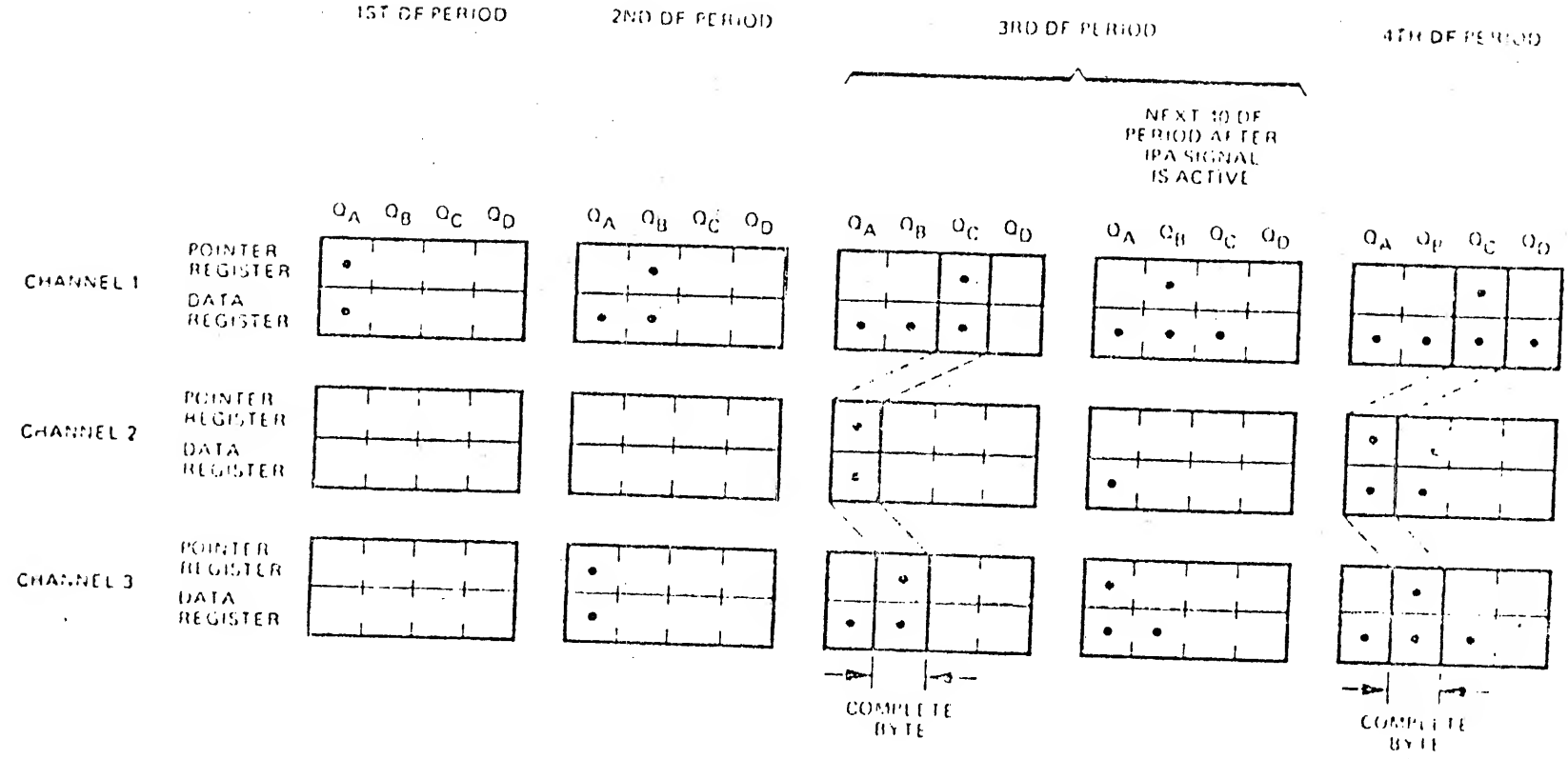
1. Skew buffer operation

The illustration represents the skew buffer method of handling skew. Each buffer has a four-bit data shift register and a four-bit pointer shift register. The data register stores up to four byte times of data. The pointer register sets a bit in the location corresponding to the next data bit to be transferred from the skew buffer and keeps track of this bit until it is transferred out.

For simplicity, assume a three-channel tape drive which is moving tape across the head assembly:

- During the first DF, channel one receives data and sets the pointer in the "A" position since this is the next data to be transferred out. Channel two and three have not yet received data because of the effects of skew.
- During the second DF period, channel one again receives data shifted into its data register. The pointer shifts to position "B" along with the first data bit. Channel three also receives data shifted into its data register and sets the pointer to the "A" position. Channel two still has not received data (possibly due to extreme head gap skew). A complete byte has not yet occurred.
- During the third DF period, channel one shifts in additional data. Its pointer also shifts to keep track of the first data bit. Channel three shifts in additional data and its pointer shifts to the "B" position. Channel two finally receives data shifted into its data register and sets its pointer in the "A" position. Simultaneously to setting the last pointer, the read control logic is notified that a complete byte is ready to transfer.
- During the next one 40th of a DF time period, the data in the register location corresponding to its pointer location is transferred to the data PCA. Then each pointer is shifted one position to the left so that it points to the next data bit in its data register. Since channel two only had one data bit stored, the pointer is removed.
- During the next DF period, each channel shifts in additional data. The pointers of channels one and three shift along with the data. Channel two sets its pointer when the data is shifted into its data register. Again, a complete byte is detected.

SKEW BUFFER OPERATION



NOTE

FOR SIMPLICITY, THE SKEW BUFFER SHOWN HAS ONLY THREE CHANNELS INSTEAD OF NINE

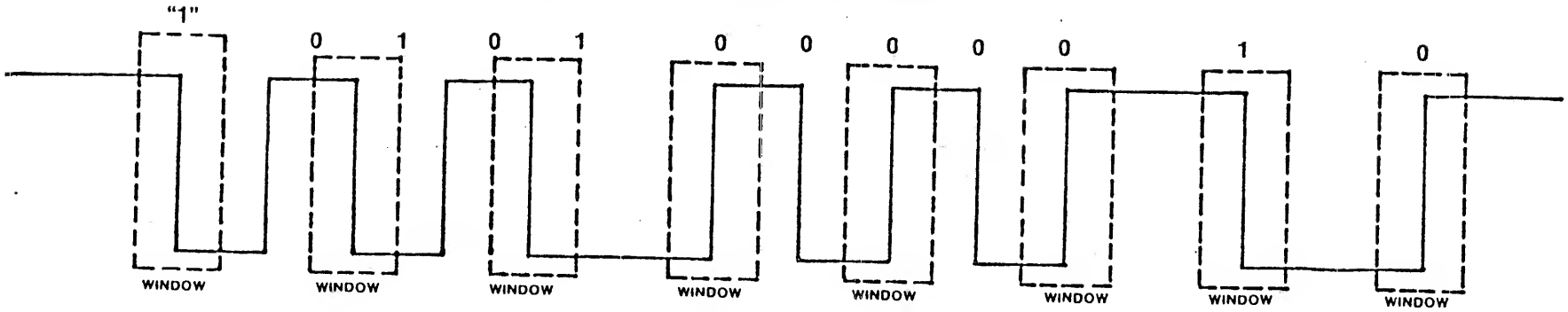
DF: DATA FREQUENCY

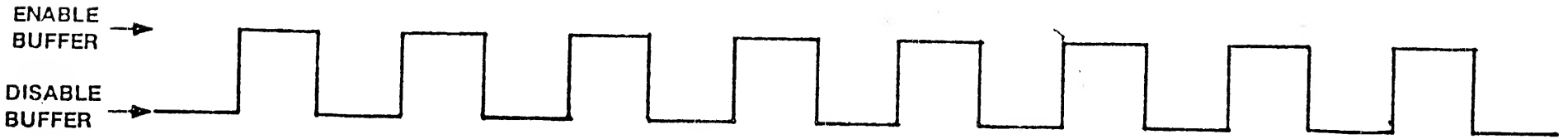
40DF : 40 × (DF)

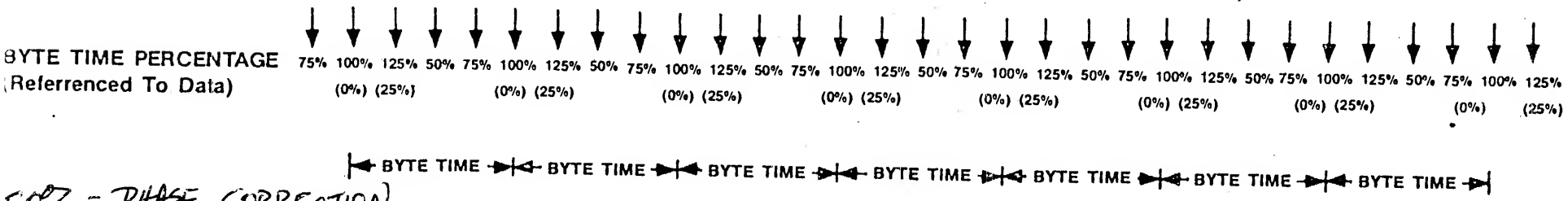
IX-B,2. Window Principle

When reading from the tape, phase correction transitions look the same as data transitions. If these phase correction transitions were allowed to enter the skew buffer, they would be interpreted as data. These transitions must, therefore, be blocked out before they reach the buffer. Phase correction transitions take place at approximately the 50% point of the byte time and data transitions occur at the zero or 100% point of the byte time. If the skew buffer is enabled only between the 75% and 125% points of the byte time, the data transitions will enter the buffer but the phase corrections will be effectively blocked.

WINDOW PRINCIPLE







50% = PHASE CORRECTION

IX-B,3. Phase Encoded Read Block Diagram

The PE read electronics is primarily contained on the decoder, data and status and read control PCA's.

The nine decoder cards are similar to nine input/output devices. They operate as nine independent devices to the read control electronics. Each card contains four storage registers which operate to provide electronic deskewing. Each receives signals from the preamplifier and read control electronics, decodes tape unit inputs and sends both level and data to the read control PCA.

In addition to the read control PCA, the read control electronics includes the data and status PCA. They provide error detection and correction, sixteen state hardware programming for data control, timing and decoding of level data (for either tape mark, IDB or any channel level). They also provide buffered outputs for signal conditioning of the read data lines and clock; and the outputs and buffering to the interface of MTE, STE, tape mark, EOB, and ID burst.

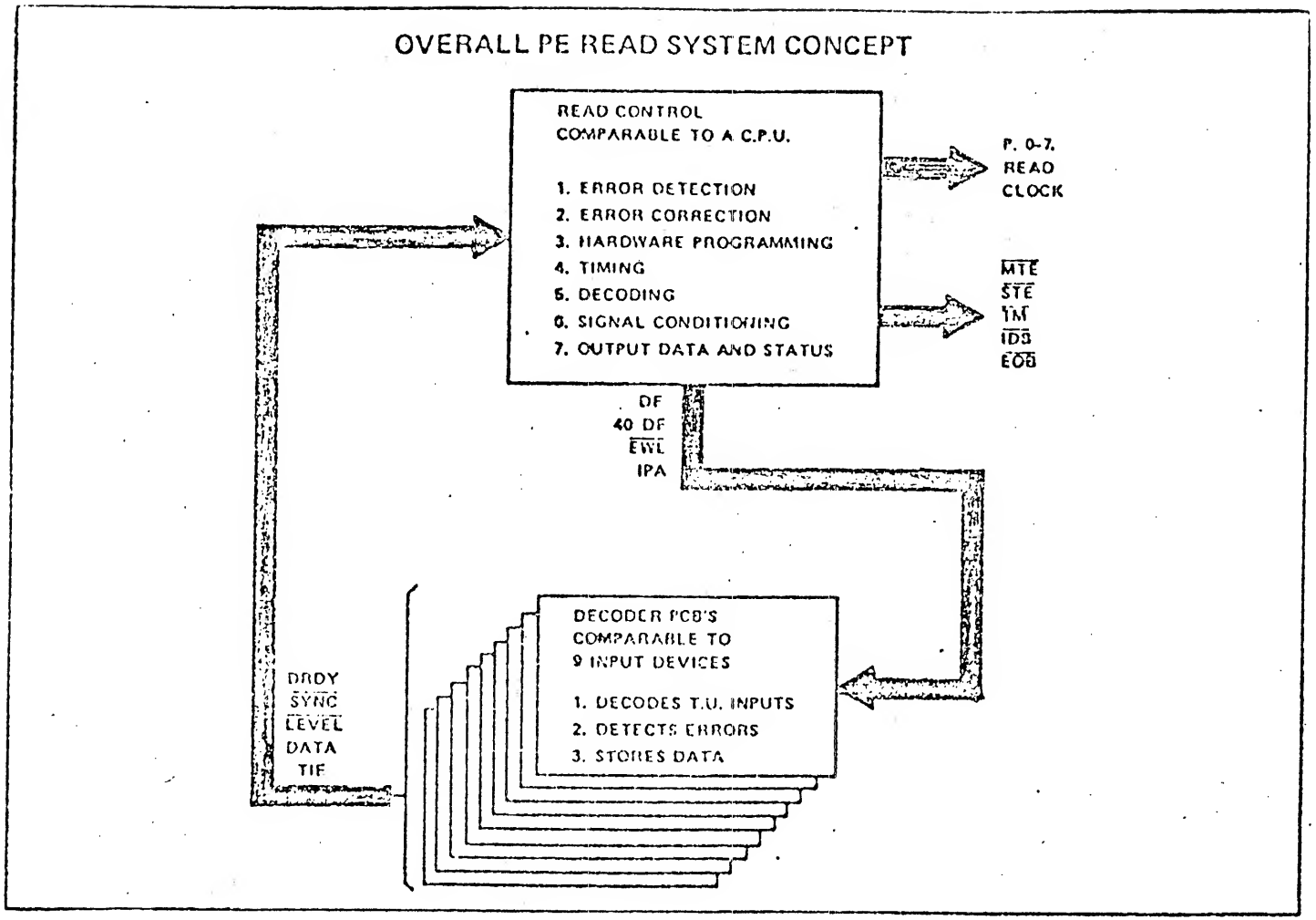
The PE read electronics block diagram contains six individual blocks:

- The master unit preamplifier PCA.
- The slave unit preamplifier PCA (identical to the master).
- The slave PE read PCA.
- One of nine decoder PCAs (the one for parity).
- The data PCA.
- The read control PCA

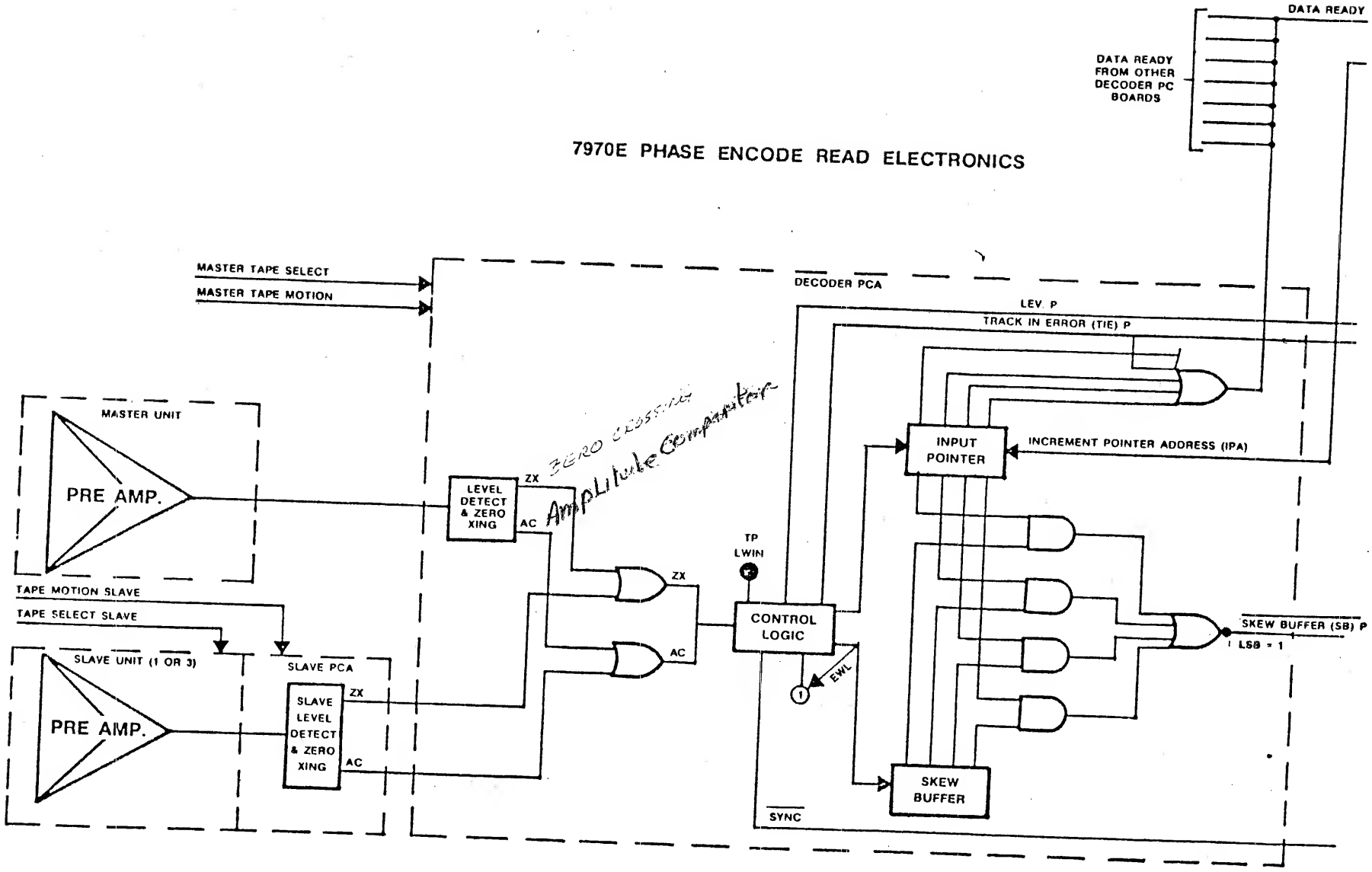
The data PCA contains the level logic, track-in-error logic, other miscellaneous logic and the data transfer registers. The read control PCA contains the combining and control logic for the read control sixteen-state decoding.

From the read head the signal from tape is applied to the input of the preamplifier. The preamplifier gain is adjustable. The output of the preamplifier feeds the decoder PCA.

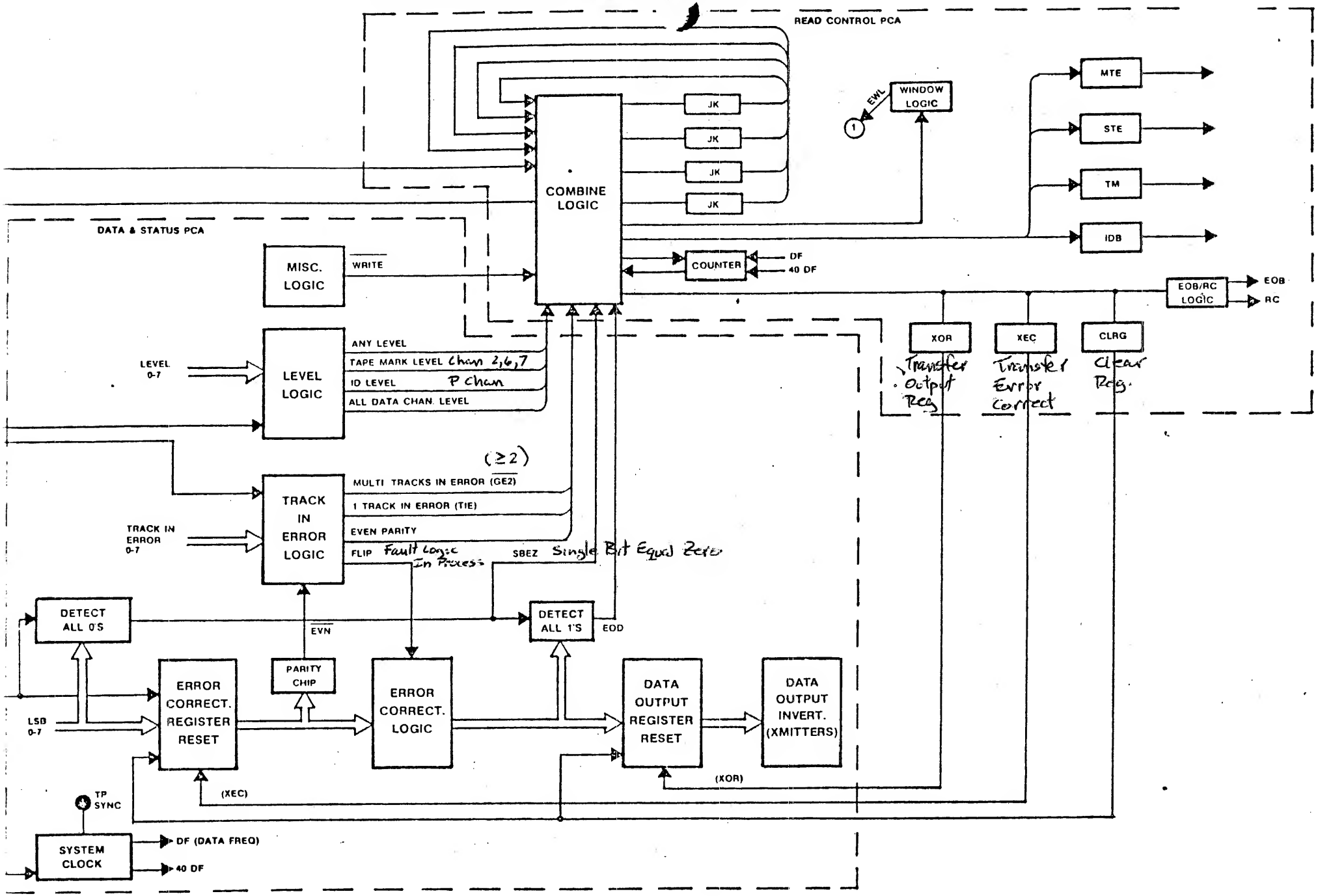
OVERALL PE READ SYSTEM CONCEPT



7970E PHASE ENCODE READ ELECTRONICS



7970E PHASE ENCODE READ ELEC[illegible]ICS



The slave ZX and AC lines represent the zero crossing and amplitude comparator signals from a slave unit. The ZX and AC signals for the master unit are derived on each of the nine decoder PCAs. The ZX and AC signals from the master and slave units are "ored" in the decoder PCA.

The control logic contains logic for several functions including the window logic, window generator, pointer register enable latch, amplitude detector and error detection logic. There are two shift registers, one for the input pointer and another for the skew buffer. This input pointer points to the data bit in the skew buffer that is ready to be transferred out. The skew buffer can store up to four characters of data. The control logic causes the pointer to point at the correct skew buffer position keeping track of the data bits as they are being transferred out into the data PCA.

The five input "or" gate at the top right hand corner of the decoder printed circuit boards provides a data ready output signal which is "nor" tied with the nine other ready lines from the nine other decoder PCAs. All nine data ready signals must be true for a system data ready to occur. DATA READY is true when any of the four input pointer positions of the input printer shift register is activated and pointing at a data bit. The fifth input into the same "or" circuit is provided so that when any decoder channel goes to Track-in-Error, data ready is true but the skew buffer output to the data PCA from the decoder PCA is also set to a zero data state, regardless of the data that was stored in the Skew Buffer. Later it will be shown that setting the Skew Buffer to zero with a Track-in-Error allows calculating the correct data if only one track is in error.

ENABLE WINDOW LOGIC (EWL) will become true when the control logic for the PE System decides that the block being decoded is a data block. This command tells the decoder PCA to begin decoding "ones" and "zeros".

The window circuitry is the electronics which distingushes data from phase transistions. When the window is open the ZX transitions that are allowed to pass through have to be data transitions. The ZX transitions are blocked when the window is closed because they are phase transitions.

There are three conditions for a track-in-error (TIE) to be set by the decoder PCA:

- during the time EL is asserted if no ZX transition occurs.
- Whenever a loss of level (AC) occurs for a count of from two to three data character times.
- When a skew buffer overflows. If the maximum storage locations of the electronics deskewing buffers are being utilized (ie, the fourth position) and another data "one" or "zero" is ready to be transferred in, an overflow would result. Thus, TIE would be asserted.

Even though it is not shown on the block diagram, any time TIE occurs, the output of the skew buffer on that particular track will go high or to the zero data condition and that data ready will go true.

INCREMENT POINTER ADDRESS (IPA) is asserted true each time a data bit has been transferred out of the decoders into the error correction register of the data PCA. The purpose for IPA is to increment the skew pointer address and pick up the next byte being constructed in the skew buffers. When all nine decoder PCA skew pointers are pointing to the next logic "one" or "zero" DATA READY will occur again. TIE also sets DATA READY.

$\overline{\text{SYNC PULSE}}$ is available on all nine decoder PCAs but it is only utilized in channels two and parity. This signal is proportional to the frequency of data coming from the tape. $\overline{\text{SYNC PULSE}}$ is used during a read only mode to ensure that system clock is proportional to the average input frequency derived from tape. It is not used during the mode of read-after-write.

Refer to the data and status PCA. $\overline{\text{WRITE}}$ is an output signal from the miscellaneous logic block. $\overline{\text{WRITE}}$ is asserted during a read-after-write mode of operation.

The level logic inputs are the nine level signals from the decoder PCAs. The outputs are as follows:

- $\overline{\text{ANYL}}$ which indicates an input on any of the nine levels.
- $\overline{\text{TML}}$ indicates active tape mark level and all other levels are inactive.
- $\overline{\text{IDL}}$ indicates that the ID channel level is active and all other levels are inactive.
- $\overline{\text{ALL}}$ indicates all data channel levels are active.

Inputs for the TIE logic are the same as for the level logic. Output $\overline{\text{(GE2)}}$ indicates an error in two or more tracks. $\overline{\text{EVEN}}$ is active when even parity occurs with no track-in-error. $\overline{\text{ET}}$ is asserted when one and only one TIE occurs. FLIP is asserted when $\overline{\text{ET}}$ is active and there is an even vertical parity detected at the output of the error correction register.

Due to the operation of the decoder card, whenever TIE is set it will stay set throughout the remainder of the data block in which TIE occurred. The skew buffer output of the decoder card will always go to zero whenever TIE occurs. During a STE, flip will be set true only when even parity occurs and it will correct only that track which is in error. Hence, there is a closed loop for a single TIE of vertical parity. Flip will only be true when there is an even vertical parity detected, even though the status is true.

The input to the detect all zeros block is the output of the skew buffers of each of the nine decoder PCAs. Whenever all the skew buffers are high or at their zero state, skew buffer ($\overline{\text{SB}}$) will be asserted. $\overline{\text{SB}}$ implies that all zeros are present for a

particular data byte at the output of the error correction logic and the gating of the detect all ones is set so that it will be true whenever an all ones byte, error corrected, is fed into the detect all ones logic block. Another input into the detect all ones block is $\overline{SB}$. Note that the output of the detect all ones block is end-of-data (EOD). Recall on the tape format that EOD occurs at the first two characters of the postamble. The first two characters of the postamble is an all ones character followed by an all zeros characters. Anytime a detected all ones character is followed by an all zeros character, EOD will be true. EOD is fed into the control logic of the read control PCA to stop data transfer.

Next, note the error correction register, error correction logic, data output register, and data output inverters. These four blocks are the means by which the data is transferred from the decoders, corrected when required, and transferred to the out-put of a controller by means of the read clock. The input in the error correction register is all nine channels of the decoder card skew buffers. Whenever a system data ready occurs the out-put of the skew buffer is loaded into the error correction register by a XEC command. XEC means load the error correction register. Since data ready cannot occur during the preamble time no preamble characters will be loaded into the error correction register. Upon completion of the XEC command vertical parity is examined on the data bit. If necessary, during a single TIE condition, flip will be set to make a correction through the error correction logic.

The first DATA READY causes the error correction register to be loaded. No data is transferred to the interface. After the second data byte is constructed, READY goes true again. Upon receipt of this second READY status, LOAD OUTPUT REGISTER (XOR) goes true. The contents of the error correction register (the first data logic) is passed through the error correction logic, corrected if necessary, and on to the output register. Shortly after the output register is loaded by the XOR command, READ CLOCK fires and transfers the data to the interface. At

the same time, the DATA READY command that caused the XOR causes a new XEC command to load a second byte into the error correction register. This sequence continues until all the data bits have been transferred through the output register into the interface by means of the READ CLOCK until EOD goes true.

When EOD occurs, there are no more XOR commands, hence the first postamble character will not be transferred out to the interface. That completes the data cycle. There will always be two more DATA READY pulses than there are data bits transferred out in order to complete the data transfer cycle.

A false EOD could occur if there is one TIE. It is possible to have a corrected detected all ones byte through the error correction logic to the detect all ones gate, and have the skew buffer output equal to zero on all channels because of the one TIE condition. Hence, if this STE occurs in a read-only mode, postamble verification takes place. Postamble verification also takes place in read-after-write mode on every block of data.

During postamble verification, $\overline{SB}$ equals zero. Status is looked at for each of the first 36 characters of the postamble. DATA READY occurs on each of these characters but XOR does not come true. Hence, postamble will not be transferred to the interface. Data transfer stops if EOD is detected whether it was really EOD or not. If at any time during postamble verification the skew buffer does not equal zero on all channels, a multiple-track-error (MTE) status would be set and the data block would either have to be considered invalid, reread or ignored. During the read-only mode, if a single TIE occurs, besides postamble verification, EWL command would stay true until the end of postamble instead of EOD time in order to verify that all the skew buffers equal zero. This will be covered in more detail later in the text.

The last block in the lower lefthand corner is a block that represents system clock. The output of system clock is DF which is data frequency and 40 DF which is 40 times the data frequency rate. The input to the system clock is SYNC from channels two and "P" decoder cards during read only mode. Channel two has priority. If, for some reason, channel 2 sync becomes inaccurate channel "P" is logically switched in to take over. During a read-only mode, the system clock, DF and 40 DF is an output which is proportional to the average of the input frequency coming from tape. During read-after-write mode, system clock, DF and 40 DF are a function of a crystal contained on the data PCA and are not controlled by SYNC.

The last large block is the read control PCA. It contains the combining logic, a general purpose counter, status outputs for MTE/STE tape mark, ID burst, EOB pulses and read clock pulses.

The combining logic contains the binary to octal decoding which provides sixteen unique outputs. These outputs are conditioned by four JK flip-flops. These sixteen outputs provide sixteen unique states. The PE read circuits are state controlled. When the machine is in any given state it is given certain directions and makes certain decisions. The results of the decisions advance the machine to another operation or another state. State control logic sequences the activities of the data path circuits during any PE read operation. The final decision is made when the proper conditions exist to generate output signals.

The PE read circuits operate in two modes; read-only and read-after-write. Signals read off tape in read-after-write mode are required to meet more stringent requirements, before being recognized as valid than read-only mode signals. This ensures reliability and compatability to industry standards. The state decoding outputs are combined to give various commands, such as EWL, XOR, READ CLOCK, and EOB. Other status outputs include MTE, STE, TAPE MARK, and ID BURST.

The basic clock for the combining logic is DF and 40 DF. The general purpose counter will either count at a DF or 40 DF rate, depending on what conditions are required. At the appropriate time, MTE STE, TAPE MARK, or ID BURST status will be set. At the end of the particular block for which status was set, EOB pulse will fire sending that particular status to the interface controller. READ CLOCK will occur at the end of each data byte.

A clear register (CLRG) signal occurs at EOB time. This is a master reset to clear out the error correction register and the data output register on the data PCA. If the output register was set true by the last data bit in a data block, that logic "one" will not be cleared out of the output register until EOB is detected.

IX-B,4. PE State Control Flow Diagram

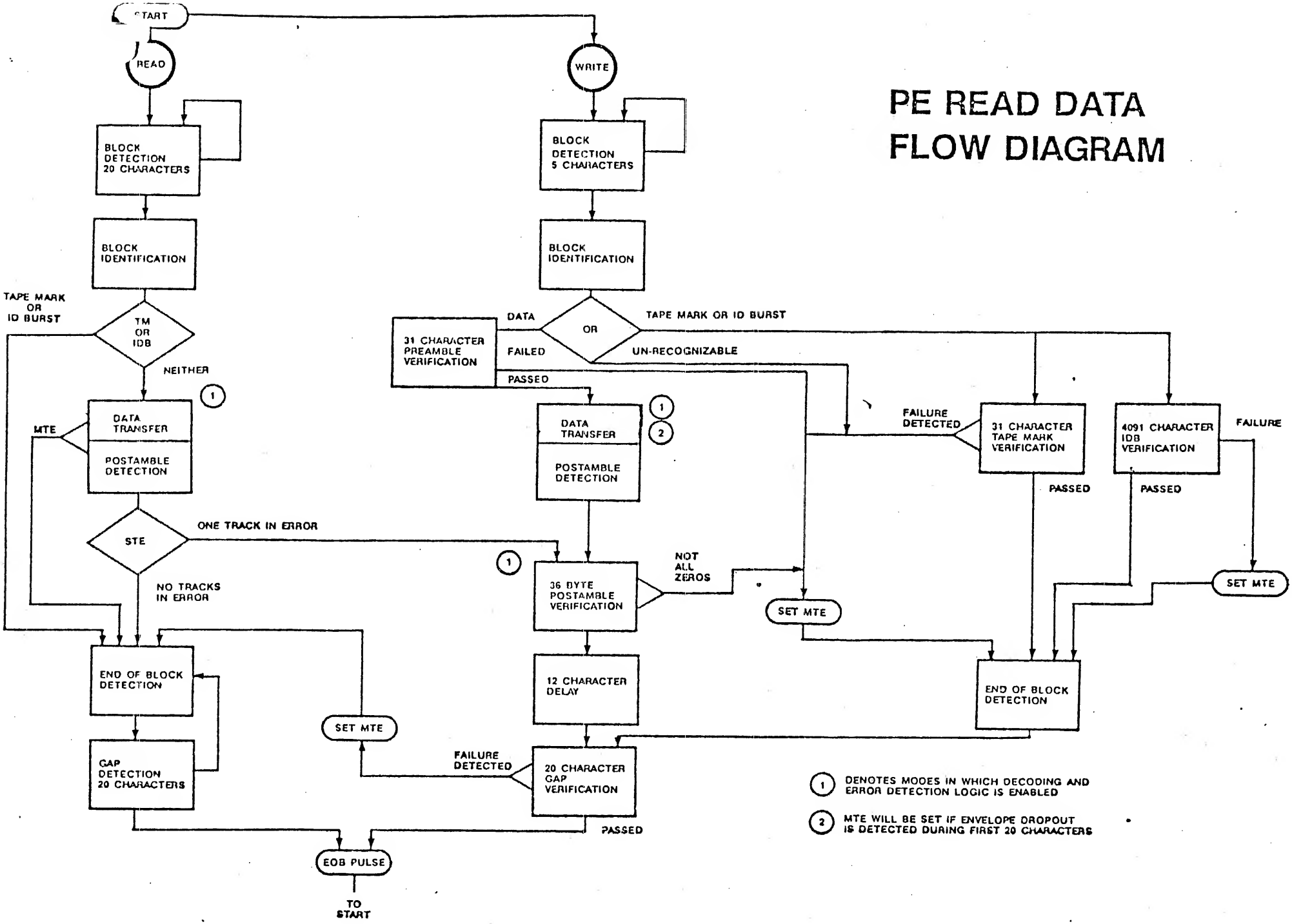
Refer to the simplified flow diagram for the PE read data electronics. After following the discussion through the simplified flow diagram, repeat using the PE state control flow diagram (figure 4-11 of the service manual).

There are two modes of operation; the read-only and read-after-write modes. The read-only mode and the difference between the read-only and read-after-write modes will be presented. In the read-only mode, the decoding electronics is not as critical of format since it is simply trying to recover the data. In read-after-write, a more extensive verification of the preamble, the postamble, the tape mark blocks and the ID blocks is performed; because while generating the tape, a more accurate check of tape format is required. The program sequence includes the following in the read-only mode:

- Block detection of 20 characters.
- Block identification of a tape mark, ID burst or data block.
- Data transfer
- The end-of-block detection
- Gap detection of 20 characters
- EOB pulse

Note the block detection of twenty characters. In order for any block to be a valid block, regardless of whether it is a data block, a tape mark block, or an ID block, it must be more than 20 characters long. A block of less than 20 characters is considered to be noise and will be ignored. Once it has been decided that the block is at least twenty characters long, a block identification mode takes place at the first qualifier; tape mark, ID burst, or neither. Assume that ID burst is the block decoded. If the IDB block was present for at lease 20 characters, the ID burst status will be set.

PE READ DATA FLOW DIAGRAM



Nothing else will happen until the end of this block has been detected. When there is an absence of level for at least twenty character times it is assumed to be the end of the ID block and the EOB pulse will be fired which will take the state back to the start and transfer the IDB status out. The same thing would happen if a tape mark block were detected. If the tape mark block had been decoded the status would be set. When the end of the tape mark block occurred, there would then be a gap detection of 20 character times and the EOB pulse would again fire and transfer out the tape mark status.

Assume the block is not a tape mark block or an IDB block, but a data block. Twenty characters into the data block, data transfer would be established and the decoder card would be enabled to start decoding data "ones" and "zeros". Data Transfer would begin after the last preamble character. During the transfer of data to the controller, if no errors occur, data will continue until the End-of-Data detection occurs. Then, at the end of the postamble and after the postamble has been absent for 20 character times, an EOB pulse will be generated by the system. If a multiple-track-error (MTE) occurs during data transfer, data transfer will immediately cease, and the read control electronics will go into an EOB detection mode and fire the EOB pulse, once again, 20 characters into the gap. If, during read-only mode an STE occurs, data transfer will continue and the track that was in error will be corrected for by examining vertical parity. Because it is possible to sense a false end-of-data, a 36 byte postamble verification and then a 12 character delay, followed by a 20 character gap verification will take place prior to firing the EOB pulse. This is to give thorough verification that the postamble was in fact a valid postamble.

Notice the qualifier STE following the postamble detection. When STE is true, the exit is to a 36 byte postamble verification block which is in the read-after-write sequence according to the block diagram. In the read-only mode, if an STE occurs

a 36 byte postamble verification will occur. If at any time during this 36 byte postamble verification, all of the skew buffers do not equal zero; MTE will be set, end-of-block detection will take place, a 20 character gap verification will take place and EOB will be fired sending MTE status to the controller. If, however, the test for a 36 byte postamble verification is passed and each of the characters are all zeros, a 12 character delay time will be generated. At the end of that time, a twenty character gap verification takes place. If it fails, an MTE will be set once again. However, if it passes, an EOP pulse occurs, and even though there was a single-track-error, it will be a good postamble verification and the record will not have to be re-read.

Consider now the read-after-write mode. During the read-after-write mode a block detection of only five characters is required before a block identification occurs. As in the read-only mode, there is a qualifier for data, tape mark or ID burst also. The data transfer and postamble detection is very much the same as in the read-only mode when an STE occurred. Additionally, the read-after-write mode has a verification, a twelve character delay and a twenty character gap verification. A more thorough test of the tape mark block and the ID burst block, and much closer examination of the preamble is accomplished during the read-after-write mode. The PE read-after-write electronics is designed to ensure correct format. During a read-after-write operation, only a five character block detection is done so that the block can be more closely examined.

Next, a block identification occurs. Assume the first character is an IDB block. After the first five characters of block detection it would set the IDB status. It would then verify that the IDB is at least 4096 characters long. If the block were not 4096 characters long, MTE would be set and then wait until the end-of-block. After EOB, it would do a twenty character gap verification and fire EOB pulse. The EOB pulse should be used to clock the IDB status and MTE status, if it occurred, and pass it to the controller. The same thing would happen if the block were a tape mark block.

If the block being detected is five characters long and it is not a TM block, an IDB block, or a data block, it would be considered an unrecognizable block. MTE would be set, the status of which would be transferred out at EOB time to the controller.

If a block is five characters long in read-after-write mode and it is a recognizable data block, preamble verification would begin. Five characters into a data block preamble, the EWL window logic is set turning on the decoder cards to start decoding "zeros" and "ones". DATA READ first occurs at the end of the preamble verification and data transfer begins. Data transfer will continue until the End-of-Data.

Automatically, then a 36 character postamble verification takes place. Next, a twelve character delay and a 20 gap verification takes place. If all the above tests are not passed, MTE would be set and that MTE status would be transferred at EOB time to the controller. During the read-after-write mode the EWL is turned off at the end of the postamble verification.

The PE read circuits are state controlled. When the machine is in any given state, it is given certain directions and makes certain decisions. The results of the decisions advances the machine to another operation or another state. State control logic sequences the activities of the data path circuits during any PE Read operation. This data path consists of the decoder, data and status, and the read control PCAs. The final decision is made when the proper conditions exist to generate output signals.

As noted previously, the PE read circuits operate in two modes: read-only and read-after-write. Signals read off tape in read-after-write mode are required to meet more stringent requirements, before being recognized as valid than read-only mode signals. This ensures reliability and compatability to industry standards.

The flow diagram is laid out and itemized to show the direct correlation of the state decisions to the logic shown on the schematics of the PCAs (refer to figure 4-11 of the Parts and Diagrams Manual). Each decision block within each state has a notation showing which PCA makes that decision, often the area on the PCA schematic is included.

When power is applied to the PE read circuits, most sequencing and output circuits are reset (state counter is reset at 0000). When a signal is detected in any of the nine channels, a check is made to determine if the PE read circuits are operating in read-only or read-after-write mode (state 00, refer to figure 4-11).

To show the use of the flow diagram in conjunction with the diagrams manual, let's say in the above decision we are in the read-after-write mode. The state counter advances from 00 to 04. Once in state 04 (S04), the next decision is: are there 5 consecutive byte times with a signal present on any channel? As shown on the flow diagram, this decision is made on the Read Control PCA and specifically in the state control logic. Now refer to the read control PCA schematic, the output of U27C nor gate is S04, count 5 (cnt 5), and signal present any channel, ANYL (S04+CNT5+ANYL). If either CNT 5 or ANYL is a

false or low signal, then this would correspond to a "NO" decision on the flow diagram. "Noring" this output (false) at U44A with the term CNT36 puts two low signals on the input and a high on the output. The high output resets U111B (2^2FF) (through NAND gate U49A) and the state count goes from 4 (0100) to zero (0000).

Now note U310A of the read control PCA. Its output is CNT5 and S04. This output goes to NAND GATE U39A and is gated with Identification signal (IDL). If this output is true, the U111A (2^3FF) is set. This is a yes decision for the first two decisions on the flow diagram in state 04. Thus, the true output (U111A) causes the counter to go from S04 (0100) to S14 (1100), as indicated on the flow diagram.

The discussion above relates the method of using the flow diagram and the schematics for detailed circuit troubleshooting.

IX-B,7 PE Read Preamplifier PCA

There are nine identical circuits for the nine channels on the read preamplifier PCA. The signal is received on Pin 5 of U1. Pin 1 of U1 is the amplified output. The gain is adjustable by a 50K variable resistor.

The amplified output is differentiated by the R-C network, and amplified by U1B. Differentiation shifts the phase of the signal by 90^{o}. Refer to the figure of PE preamp digital signals. At the peak of the preamplifier signal (U1A), the output of U1B is passing through zero. The top of the figure shows the flux on tape. The next two signals are the preamplifier and differential outputs, respectively.

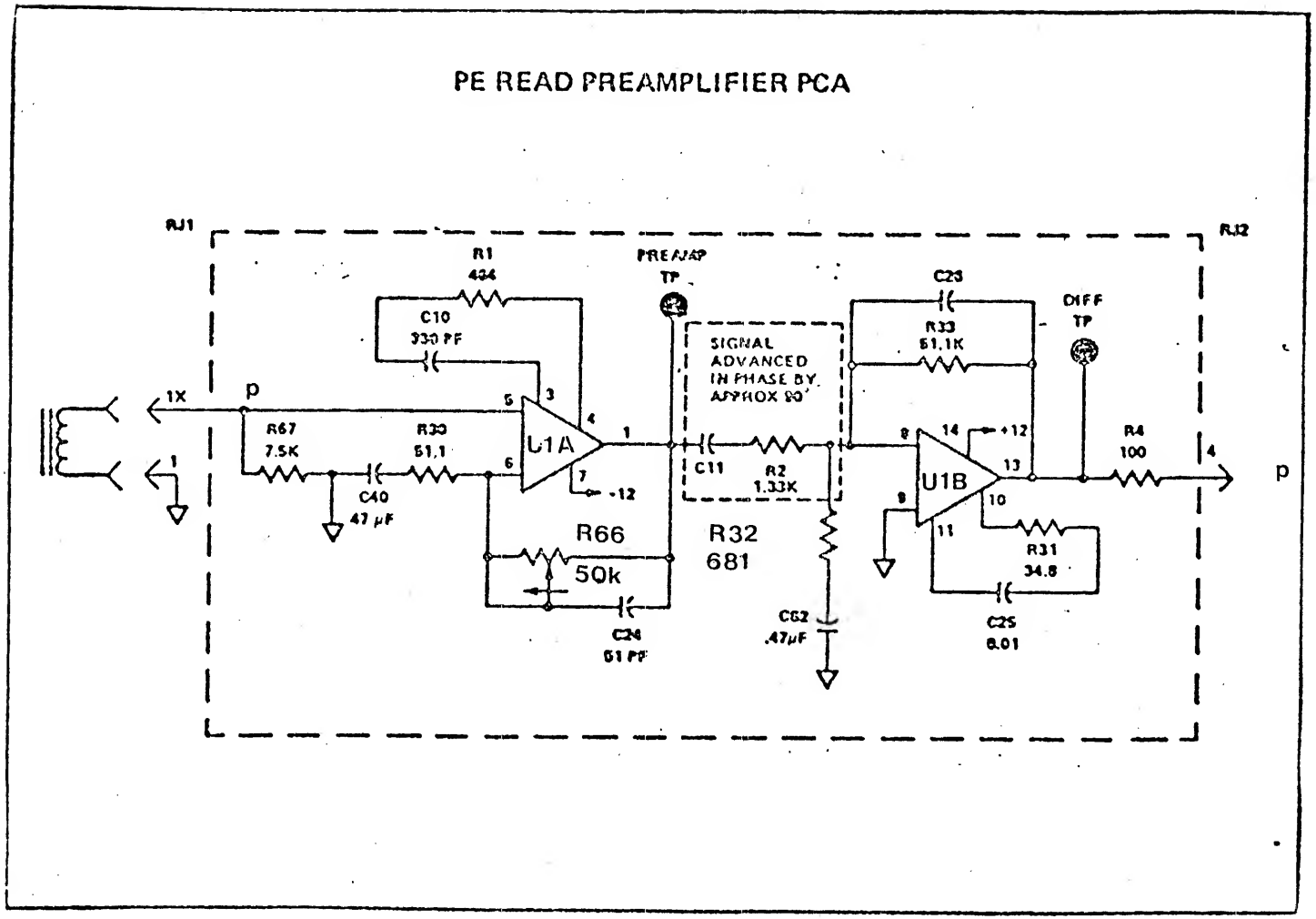
The output of the differentiator is fed through a zero crossing detector called the (ZX) zero crossing data output. The output of the zero crossing detector changes state each time the differentiator passes through zero. Since the differentiated signal passes through zero at the peak of the preamplifier output, it will always occur at the peak of the preamplifier output regardless of the amplitude, hence, amplitude instability has no effect on the zero crossing output. The output of the zero crossing detector is a digital signal representing the data one and zero, and the phase pulses.

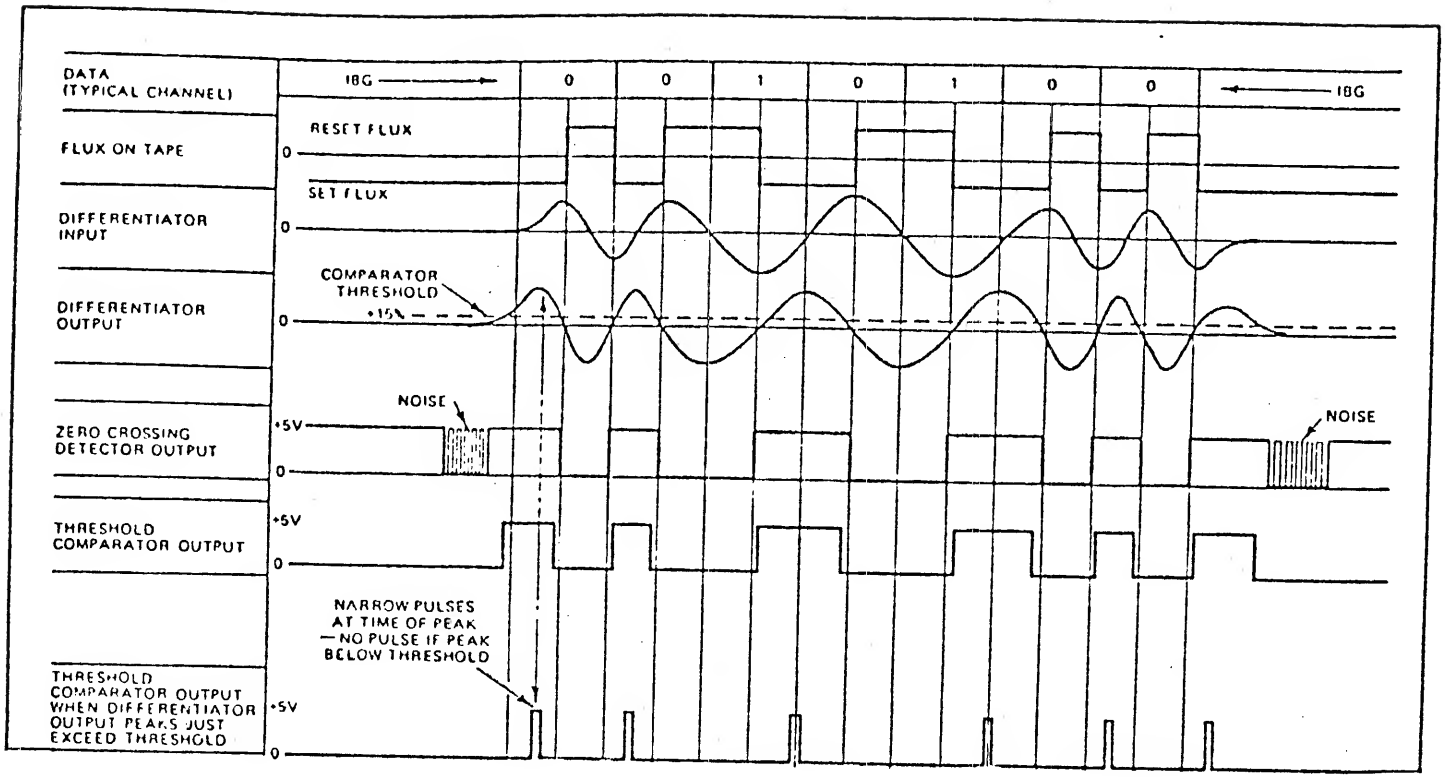
At the differentiator observe a dotted line which represents the threshold level of 15%, which is a typical threshold for read-only mode. The read-after-write threshold is 35%.

The last two outputs amplitude comparator (AC) are digital signals proportional to the amount of the differentiator output which is above the threshold level. The negative portion of the AC pulse is proportional to that amount of signal which is above the threshold at the differentiator output. The first amplitude comparator signal is well above the threshold, hence, a very long duration of negative pulse.

The lower amplitude output represents a very narrow negative pulse indicating a very slignt (above threshold) condition at the differentiator output. The amplitude comparator signal is used by the PE read control electronics. For data block, ID block, and TM block information.

The preamplifier gain is set by adjusting R66 while monitoring the DIFF test point with the tape drive writing at 1600 FRPI density.


PE READ PREAMPLIFIER PCA
RJ1
RJ2
R1
434
C10
330 PF
PREAMP
TP
C23
R33
51.1K
DIFF
TP
SIGNAL
ADVANCED
IN PHASE BY
APPROX 90°
1X
p
R67
7.5K
R30
51.1
U1A
C40
47 µF
-12
C11
R2
1.33K
R66
50k
R32
681
C24
51 PF
C62
.47µF
U1B
+12
R4
100
R31
34.8
C25
0.01
p



PE DIGITAL WAVEFORMS

IX-B,8 Slave PE Read PCA

The purpose of the slave PE read PCA is to provide digital signals for zero crossing data (ZX) and amplitude compare (AC). It also provides slave tape unit status, write mode ($\overline{WSI}$), tape motion synchronous reverse ($\overline{REVI}$), and slave unit PCA selcted ($\overline{SPE}$).

All nine data channgels from the slave preamp are fed to the slave PE read PCA. Each data channel has its own circuitry. That is, there are nine unique amplifier/gate combinations that are independent from each other. Each data channel is fed through a comparator to provide a digital signal (AC) whose low duration represents the amount at the differentiated signal which is above threshold. The threshold is either 15% in read-only mode or 35% in read-after-write mode. Read-after-write mode is activated by WRITE LATCH status ($\overline{WL}$). Both ZX and AC are anded with tape motion.

DENSITY 1600 is "anded" with SOLB to provide SPE status to the master PE read control electronics. SPE enables the master read electronics to be used by the slave. As long as power is applied to the master, it can be used by the slave even if it is off-line.

For the following discussion, refer to page 2 - 96A in the Diagrams and Parts Manual.

There are nine decoder PCA'S in the 7970E read logic (one PCA for each channel). The differentiated output from each channel's associated pre-amplifier is routed to the read data input of that channel's decoder by the read mother board. This differentiated signal is applied to the inputs of the zero crossing detector and the threshold comparator.

The negative input voltage of the threshold comparator is set by the data and status PCA. This voltage will be + 0.3 Vdc during a read-only operation and + 0.78 Vdc during a read-after-write operation. The positive input line of the threshold comparator is presented with the differentiated input signal. The threshold comparator will provide a high level output during the time the differentiated signal level exceeds the + TH level set by the data and status PCA. If MASTER READ ENABLE (MREN) from the data and status PCA is active, the threshold comparator's output is inverted and applied to the $\overline{MR}$ input of the amplitude detector. MREN will be active if the master tape drive is selected, on-line, and has motion. If a slave is selected, on-line, and has motion; MREN will be inactive and the $\overline{\text{AMPLITUDE COMPARISON}}$ ($\overline{AC}$) signal from the slave PCA will be applied to the MR input of the amplitude detector from pin 1X of this decoder PCA.

The amplitude detector functions as a shift-register and is clocked by a clock pulse from the data and status PCA. This clock is running at data frequency (DF). In other words, it clocks at byte time intervals. During normal operation the $\overline{\text{AMPLITUDE COMPARISON}}$ ($\overline{AC}$) will be low during the DF clock pulse providing a low level signal at the Q2 output of the amplitude detector. This signal is inverted to present a high level true signal at the LVL test point, then again inverted and sent to the data and status PCA as $\overline{\text{LEVEL}}$ ($\overline{LV}$). In the data and status PCA it is used to decode $\overline{ALL}$, $\overline{TML}$, $\overline{IDL}$, or $\overline{ANYL}$ for use in the read control algorythm. On channel two it is also used to switch the clock sync to "P" channel in the event that channel two has lost level. If the $\overline{AC}$ signal is not active during the DF clock, a high level will be clocked into the first position (Qo) of the amplitude detector. Each DF clock pulse will shift this level one position

until at the third DF clock pusle the high level will be present at Q2. If AC becomes active before the third DF clock pusle it will clear this high level signal before it reaches the Q2 output. However, if AC remains inactive for three consecutive DF clock pusles the high level signal present at the Q2 output of the amplitude detector will signal loss of level to the data and status PCA. Also it will set the track in error flag (TIE) through the error detection latch if enabled. Error detection will be considered later in this section.

The zero crossing detector will output a level change for each zero crossing at its input. If MREN from the data and status PCA is active, the zero crossing detector output is applied to one input of an exclusive-or gate. MREN will be active if the mater tape drive is selected, on-line and has motion. If a slave is selected, on-line, and has motion; MREN will be inactive and the zero crossing detector output from the slave PCA will be presented to the exclusive-or gate from pin 2 of this decoder PCA.

The exclusive-or circuit works as a selective inverter so that if the tape unit MASTER REVERSE (MREV) from the data and status PCA becomes active, the output from the exclusive-or circuit (which is the DAT test point) will be inverted. This inversions compensated for lines of flux being crossed in the opposite direction during reverse tape motion. Both master and slave, if selected, have the capability of activating MREV.

At the DAT test point a high level to low level transition will represent either a "one" or a phase correction transition. Conversely, a low level to high level transition will represent either a "zero" or a phase correction transition. This information is presented to the level change register.

The level change register is comprised of two stages of "D" type flip-flops. The second stage follows the first by 1/40th DF. The Q output of stage one is the data line to the "SR" input of the skew buffer data register. The level of this line will be shifted into the data register, if the data register's "SO" input is high. The "Q" output of both stages is fed to an exclusive-or gate. This pulse is inverted and routed to pin 5 X as $\overline{\text{SYNC}}$ $\overline{\text{PULSE}}$. If this decoder PCA is in channel 2 or P position the SYNC PULSE signal will be routed to the clock circuits on the data and status PCA by the read mother board. This allows the clock to sync to the average data

frequency during read-only mode. This is done only if the read control algorythm enters state (01) as discussed earlier. The Q and $\overline{Q}$ outputs of both stages of the level change register are fed as qualifiers to the "ones" and "zeros" gates in the window logic circuit.

Notice in the window generator, pointer register enable latch and error detection circuits a signal called enable window logic (EWL). These circuits are all inactive until EWL becomes true. From the read algorythm for the read control PCA note that this signal is activated 20 characters into the preamble during read-only or 5 characters into the preamble during read-after-write. EWL is turned off in the read-only mode when the postamble is detected if there is no track in error. If a single track is in error (STE), EWL turns off after the first 36 bytes of the postamble is verified. In the read-after-write mode, the first 36 bytes of the postamble are verified before deactivating EWL. In both modes, multiple track-in-error flags (MTE) will immediately disable EWL.

If the byte time starts with a data transition and ends with the next data transition, then any phase correction transition would take place at the 50% point of the byte time. Looking at the skew buffer data register, note that data present at the "SR" input is only shifted into the data register if the "SO" input is high. The "SO" input can only be activated by a high level output from either the "ones" or "zeros" gate. If these gates are deactivated during the 50% point of a byte time, it will effectively block phase correction transitions from entering the skew buffer. Notice that one qualifier for each of these gates in the window logic circuit comes from the window generator.

The window generator is a preset counter. The first stage is a decade counter being clocked at a 40 DF rate. The overflow of the decade counter clocks the binary counter with a 4 DF clock. Since the binary counter is clocked 4 times during a data period, each count on the binary counter represents 25% of a byte time. If the window generator were to start with a count of 5, count 5 would represent 0% of the present byte time, count 6 would occur at 25% of the byte time, count 7 at 50%, count 8 at 75%, count 9 at 100%, and count 10 would be 25% of the next byte time.

Using this count sequence, observe the Q2 and Q3 outputs of the binary counter in the window generator. These outputs allow activation of the "one" and "zero" gates in the window logic circuit during counts 8, 9, and 10. They also hold these gates inactive during counts 5, 6, and 7.

It was stated earlier that the window logic gates are first allowed to activate with a count of 8 and that a count of 8 corresponds to the 75% point of a byte time. Since no shift was allowed to occur during the 50% point, any phase correction transition was not shifted into the skew buffer data register. Data transitions are normally expected to occur at the 100% point of the byte time. This corresponds to count 9 on the window generator. Count 9 will allow a shift to occur. Whether it comes from the "one" or "zero" gate, shift will be active at the "SO" input of the data register causing what ever level is present at the "SR" input to be shifted into the data register. Notice that when shift occurs, $\overline{\text{SHIFT}}$ is fed back to $\overline{\text{PARALLEL ENABLE}}$ (PE) on both counters. This will preset the counters back to a count of 5 when the data transition occurs. The normal count sequence is 5, 6, 7, 8, 9; then $\overline{\text{SHIFT}}$ returns the count to 5. If the data transition occurs late in the byte time it will also allow count 10 to occur. Optimumly, the data transition and count 9 occur simultaneously. Even if the data doesn't cause the shift to occur until count 10, the window would still be closed for 25% before and after a phase correction transition.

The window follows the above sequence with the exception that the count is altered slightly to compensate for timing considerations and compatability with marginal tape drives. If the preset count is changed to 5.2 instead of 5, the window still opens at count 8. It will remain open until a count of 10.3 is reached. If no data transitions occur prior to count 10.3 a track-in-error (TIE) flag is set.

The two signal lines "nanded" together at the inputs to integrated circuit U35B in the lower right-hand corner of the schematic are decoded counts. One line represents count 8.3 and the other line represents count 2. Combined they represent count 10.3.

For the window to function properly, it must be synchornized with the beginning of the byte time. Initially, both counters are held to a

count "0" because EWL signal from the read control PCA is not active. Notice that when the binary counter is set to "0", the "ones" gate in the window logic circuit is held closed. However the "zeros" gate is allowed to pass transitions which will shift zeros into the skew buffer and develop $\overline{PE}$ through $\overline{SHIFT}$. $\overline{PE}$ will not preset the counters to 5.2 because EWL is not active and the counters are held to zero. The counters will first start counting when EWL becomes true and $\overline{PE}$ presets them to a 5.2 count. EWL comes true 20 characters (read-only) into the preamble and the next "0" character of the preamble activates $\overline{PE}$. The counters will then start counting synchronized to the beginning of the 21st byte of the preamble and read-only mode or the 6th byte of the preamble in read-after-write mode.

The window logic is now blocking phase correction transitions and allowing zeros in the preamble to be shifted into the skew buffer data register. These zeros have no data significance since a pointer has not yet been set in the skew buffer pointer register. Notice that the shift signal ("SO") at the data registers input is also applied to the "SO" input of the pointer register. However, the pointer register is held cleared because the enable latch has not yet been set. The pointer register enable latch will set when the first "one" bit passes through the window. This occurs in the last byte of the preamble. Notice that the pointer register enable latch is clocked by $\overline{40DF}$. The short delay between 40DF and $\overline{40DF}$ allows us to set the latch, removing the clear from the pointer register after the shift signal has been removed from the "SO" input of the pointer register. This means the last byte of the preamble will set the latch but will not set a pointer. The pointer register enable latch once set, will remain set as long as EWL remains active.

The last byte of the preamble enabled the pointer register. The next data bit that passed through the window, (this will be the first data bit of the record) will cause a shift signal which will shift the "SR" input of the data register into position "A" and simultaneously set a pointer in position "A" of the pointer register. Notice that all positions of the pointer register are "NOR" connected to the LRDY test point. A pointer set in any position will cause the LRDY test point for this decoder PCA to remain low. A low level on the LRDY test point

signifies that this channel has data in its skew buffer. LRDY is passed through a nand gate to the data ready (DRDY) buss. This buss is a "wire-or" connection to the same point on all nine decoder PCA's. Any one decoder PCA which does not have a pointer set (no data in its skew buffer) will hold the DRDY signal low. If this is the case, the next data bit which passes through the window on this decoder PCA will shift into the data register and cause the pointer to shift to position "B" in the pointer register to keep track of the first data bit. When all nine channels have set their pointers the data ready bus (DRDY) will go high, signaling the read control PCA that a complete byte is ready to pass on to the data and status PCA.

Notice that the comparator located between the data and pointer registers is configured such that, the data corresponding to the pointer position is inverted and always present as $\overline{SB}$. $\overline{SB}$ can be observed at the LSB test point. This line will be high for a zero bit and low for a one.

When DRDY becomes true, signifying that all nine channels have data ready, the read control PCA will activate a line on the data and status PCA which will cause the error correction register to latch in the data presented on each $\overline{SB}$ line. The read control PCA will then activate the increment pointer address (IPA) signal. IPA is routed to the "SI" input on the pointer register of all nine decoders. IPA will cause the pointers to shift left and point to the next data bits in their respective data registers. The process repeats as earlier described, with SHIFT causing data and pointer to shift right and IPA causing the pointers to shift left. In the event that IPA and SHIFT are coincident, both the "SO" and "SI" inputs of the pointer register would be active, causing the pointer to remain where it is and allowing the data to shift right to match the pointer. Also notice that position "D" of the pointer register and SHIFT are nanded together. A shift while the pointer is in position "D" would cause unused data to be shifted out of the data register. This would be a skew buffer overflow which would flag TIE.

The error detection circuit is the last part of Logic to be considered on the read decoder PCA. This latch is first enabled by EWL, which becomes active during the preamble. Once enabled, TIE can be set by

three conditions we have already discussed. In summary these conditions are as follows:

- Loss of level for three consecutive byte times,
- Window generator reaches a count of 10.3, and
- Skew buffer overflow.

Once TIE is set, it will remain set for the rest of the data block or until EWL is deactivated. Setting the TIE latch will cause the "Q" output to send a high level true TIE signal to the data and status PCA, signifying that this channel is in error. The $\overline{Q}$ output of the latch will clear the skew buffer data register and hold it clear for the rest of the data block, causing this decoded PCA to pass only zeros for the rest of the record. The $\overline{Q}$ output of the latch also causes this decoder PCA to always signal it has data in its buffer by acitvating DRDY for this channel.

For the follwoing, refer to the schematic diagram on page 2-97 of the Diagrams and Parts manual.

During initial power-on reset the read control PCA will activate the CLEAR REGISTERS ($\overline{\text{CLRG}}$) line at P2, pin 4X on the left side of the diagram. $\overline{\text{CLRG}}$ being activated, clears the error correction and output registers. During each inter-record gap the read control PCA will agin clear these registers coincident to signaling end of block (EOB) to the interface, (state 11 count 20 in the read algorythm).

On the right of the schematic diagram, notice the output gates. The qualifier for these gates to present data on the interface lines is TRANSFER ENABLE (XEN). It will be shown later where this signal is developed. XEN is also used as a qualifier for the flags passed to the interface from the read control PCA. Anytime the master or any slave is on-line and selected, XEN will be active (true).

On the left side of the diagram notice that the $\overline{\text{SB}}$ outputs from all skew buffer data registers are always presented to the inputs of the error correction register. When the read control PCA receives DTRDY on the nine decoder bus, it activates transfer-to-error correction register (XEC) at P1, pin 6X on the left side of the diagram (XEC occurs the first time in state 07 and thereafter in state 02 of the read algorythm). XEC causes the error correction register to latch what is present on its input lines.

The contents of the error correction register is presented to the error correction circuits and the parity checker. If parity checks good, the AGREEMENT line will be high. AGREEMENT is inverted by the nor gate to present all the nand gates at the bottom of the error correction circuits with one low level qualifier. The other input to each nand gate will also be low because its respective TIE line has not been set. Each nand gate will then hold one input of its associated exclusive-or gate high. This causes the contents of the error correction register to be inverted as it is presented to the data test points and the output register's input. At the "P" and "0" through "7" test points a high

level represents a "1" bit and a low level represents a "zero" bit. The exclusive-or circuits in the error correction circuit function as selective inverters which normaly invert. On the lower right side of the diagram is the single and multiple track-in-error decoder. If any decoder PCA sets a TIE flag, the high level TIE signal will be passed by the or gate string to the STE nor gate. If only one TIE is set, the $\overline{E1}$ signal will be set low, this notifies the read control PCA that a single track error was detected. If more than one TIE exists the nor gate associated with the highest numbered track-in-error will set the $\overline{GE2}$ line low and prevent $\overline{E1}$ from going low. This will signal the read control PCA that a MTE occurred.

Consider now the automatic correction of a STE. Recall that when a read decoder PCA sets its TIE flag that it also holds its data register cleared and holds DTRDY active. Recall also that one TIE is set, it remains set for the rest of the data block. Looking at the nand gates which control one input of the exclusive-or circuits in the error correction circuits, note that one input of the nand gate associated with the channel-in-error will be set high by the TIE signal coming from that channel. If $\overline{E1}$ is active low and AGREEMENT is also low (verticle parity error), the other input of all nand gates will be set high. The nand gate associated with the track-in-error will then have both inputs high and drop its output low. This allows the data on that channel to pass through the exclusive-or circuit without being inverted while all others are inverted. If AGREEMENT had been high (good verticle parity), the line connecting to one input of all the nand gates would have been low and the output of the nand gate associated with the channel which set TIE would have been high. This would cause that channel's data to be inverted along with the others. Once a channel sets TIE, that channel's data will be passed through the exclusive-or gate as determined by the parity checker.

If AGREEMENT from the parity checker is low (parity error), yet no channel has set TIE, and $\overline{E1}$ is not active; $\overline{EVEN}$ is sent to the read control PCA to indicate an uncorrectable error or malfunction in either the parity checker or STE-MTE decoder.

Note that the corrected contents of the error correction register is always presented to the inputs of the output register. The next data control signal from the read control PCA is transferred into output register (XOR). This occurs in state 12 of the read algorythm. Once data is in the output register, it is presented to the interface through the inverting output gates. When this data is ready to be latched into the interface the read control will issue a read clock ($\overline{RC}$) to the interface. This causes the interface to latch the data. $\overline{RC}$ is set by the read control PCA in state 16 of the read algorythm. The continuing data movement sequence is as follows; $\overline{RC}$, wait for DTRDY, XOR, XEC, $\overline{RC}$, etc. The cycle will continue to repeat until the end of the data block is detected. Note that XOR and XEC are synchronized to 40DF.

Recall that the postamble format is one all "ones" byte followed by forty all "zeros" bytes. Recall also that the inputs to the error correction register is low-level true and the inputs to the output register are high-level true. The $\overline{SB}$ lines, while waiting to be transferred to the error correction register, are presented to the skew buffer output sensing circuit. If these $\overline{SB}$ lines are all set to zero (all high) $\overline{\text{SKEW BUFFERS EQUAL ZERO}}$ ($\overline{SBG2}$) will be activated and sent to the read control PCA. Also one qualifier is sent to the end-of-data logic which is also monitoring the inputs of the output register. If (at the same time) the error correction register contains an all ones byte, the inputs to the output register will all be set to high levels, and EOD will be set active to the read control PCA. All ones in the error correction register with all zeros on the next byte corresponds with the first two bytes of the postamble.

For the discussion below, refer to page 2-98 in the Diagrams and Parts Manual.

Note on the left side of the page that DENSITY 1600 (DI6) from the preamp is anded with SELECTED and ON-LINE (SOLB) from the control and status PCA. The output of this and gate is inverted twice and sent to the read control PCA as XEN to qualify the flags from the read control PCA to the interface. XEN is also routed to the data output gates on the data and status PCA as seen on the previous diagram. If the slave were selected instead of the master, XEN would be activated by

$\overline{\text{SLAVE PHASE ENCODED}}$ ($\overline{\text{SPE}}$) from the slave read PCA.

Recall that MASTER READ ENABLE (MREN) was used on the decoder PCA's to select the amplitude comparator and zero crossing detector outputs in the master drive. Note here that MREN is active if the master drive is ready, selected on-line and has any motion command. Otherwise, MREN is inactive.

MASTER REVERSE (MREV) is used in the read decoders to invert data during reverse tape motion. Note here that MREV can be set active either by a reverse synchronous motion command from the master control and status PCA or $\overline{\text{REV1}}$ from any slave read PCA. It is otherwise inactive.

On the top left side of page 2-98 is the master drive's threshold generator. The + TH line is routed to one side of the amplitude comparator in each of the read decoder PCA's. In earlier versions of the read decoder PCA's the - TH is also used. In normal synchronous read-only mode the threshold levels are set to + and - 0.3 Vdc. Any highspeed motion command will cause the threshold levels to raise to 1.2 Vdc by turning off Q1. During read-after-write mode $\overline{\text{WL}}$ will be set active low by the write control PCA in the master write card cage. This signal will pass through nand gate U28 and raise the voltage level at the junction of R25 and R26 in the threshold generator causing the threshold levels to be set to 0.78 Vdc. Since $\overline{\text{WL}}$ and $\overline{\text{WSI}}$ from the slave can never both be active at the same time, $\overline{\text{WL}}$ will also pass through and gate U27 setting $\overline{\text{WRITE}}$ active to the read control PCA, and to the clock control circuit on the data and status PCA. The read control algorythm tests the $\overline{\text{WRITE}}$ signal during state 00 and again in state 17. The clock control circuit uses the $\overline{\text{WRITE}}$ signal to insure that SYNC is disabled during write mode. If $\overline{\text{WSI}}$ from the slave read PCA were active instead of $\overline{\text{WL}}$, the $\overline{\text{WRITE}}$ signal would be set active in the same manner. $\overline{\text{WSI}}$ would also raise the master threshold levels, but this serves no useful purpose since the slave uses its own amplitude comparators.

The right side of page 2-98 shows the active channel logic. Level signals are being applied to the active channel logic from the amplitude detectors of all nine read decoder PCA's. The active channel logic can decode four signals which are not passed through the skew buffers. These

signals are described below.

- $\overline{\text{ANYL}}$ - will be active if any channel has a low true $\overline{\text{LV}}$ signal. This signal is passed to the read control PCA and used in the read algorythm.
- $\overline{\text{ALL}}$ - will be active if all channels have a low true $\overline{\text{LV}}$ signal. This signal is passed to the read control PCA and used in the read algorythm.
- $\overline{\text{IDL}}$ - will be active if only the parity channel has a low level true $\overline{\text{LV}}$ signal. This signal is passed to the read control PCA to be used in the read algorythm. It is also passed from the read control PCA to the interface as an ID burst flag.
- $\overline{\text{TML}}$ will be active if a TAPE MARK (TM) signal is decoded. This signal is passed to the read control PCA to be used in the read algorythm. It is also passed from the read control PCA to the interface as a TAPE MARK flag.

There are two options for the tape marks. With the jumper installed in position 1 to 2, the TAPE MARK occurs in channels 2, 6, and 7. If the jumper is installed in position 1 to 3, the TAPE MARK occurs in channesl 0, 2, 5, 6, 7 and P (all HP systems are strapped 1 to 3). For either case, channels one through four must be inactive.

Refer to page 2-99 in the Diagrams and Parts manual for the discussion below.

In the lower left corner of the diagram is the clock control circuit. If $\overline{\text{WRITE}}$ is inactive high and SYNC ENABLE from the read control PCA becomes active high (this occurs upon entering state 01 in the read algorythm), $\overline{\text{SYNC PULSE 2}}$ will be inverted and allowed to act as SYNC to the clock circuits. This will synchronize the clocks to the average data frequency on channel two. Should channel two lose level or set its track in error flag, the synchronization will switch to the parity channel. During read-after-write mode, $\overline{\text{WRITE}}$ is active low and SYNC ENABLE is inactive low thereby defeating synchronization.

The basic clock is a 17 MHz crystal oscillator which is divided down by a series of decade and binary counters. Since a 1600BPI density recorded tape has a lower data rate at lower capstan speeds, a dip jumper is provided and must be inserted in the position corresponding to that capstan speed. An illustration of the jumper position for each capstan speed is provided at the bottom of the diagram. The division of the basic clock is determined by the position of the jumper. The 45 IPS position provides the least amount of division. Each slower speed provides progressively more division. To make these clock cables compatible with all speeds, the clock outputs have been labled DF and 40DF. Note that DF is always synchronized to 40DF. These clocks are routed to the read control PCA and to all nine decoder PCA's. Also, 40DF is routed to other circuits on the data and status PCA. The 45 IPS tape drive is by far the most numerous 7970E in the field. The DF clock frequency for 45 IPS is 72 KHz with 40DF being 288 KHz.

X-A PE Test Tape

The PE read data test tape (HP part number 5080-4555) is a 1200-foot prerecorded tape which can be used for performance testing and troubleshooting of the PE read circuits. It is divided into four sections by BOT and EOT reflective tabs. Section one is the only section that will be considered here.

Section one is a 450-foot section of nine-byte single-rotating bit pattern blocks. That is, each byte contains eight "0" bits and one "1" data bit. The "1" data bit occurs once in each channel per block. The primary purpose of this section is to verify data recovery, data transfer, and data block detection.

Install the control and status PCA, HP part number 13191-60010, and read data test PCA, HP part number 13196-60000, in the tape drive. Install PE data test tape, HP part number 5080-4555, in the tape unit and position the tape at the load point of section one.

Use the CF switch on the control and status test PCA to set the tape in forward motion and check (on the read data test PCA) that the RC, EOB, and SD16 indicators are on and the MTE, STE, IDB, and TM indicators are off. Connect the oscilloscope channel A probe to the parity channel preamplifier DIFF test point and adjust the sweep rate so that the block occupies 8cm. Connect the trace B probe to the EOB test point on the read display test PCA. A single pulse should be present within $\pm$0.3cm of the 10cm line (approximately 22 to 24 byte times from the end of the data block) on the scope. Set the sweep rate to 1ms and the mode to chop.

Connect the channel A oscilloscope probe to the RC (Read Clock) test point on the read data test PCA. Adjust the oscilloscope sweep as necessary to verify that nine RC pulses occur for each zero volt line crossing of the signal on trace B. The RC pulse should be a negative pulse ($\overline{RC}$) with a duration of 2.5$\pm$0.5ms (use delayed sweep).

Connect the channel B oscilloscope probe to the P data bit test point on the read data test PCA. Adjust the scope so that the spacing between the $\overline{RC}$ pulses is 1cm and the negative-going edge of the $\overline{RC}$ pulse is at the first scope graticule line. The waveform at the P test point should be a negative pulse 1cm wide. It should begin at the same time as the $\overline{RC}$ pulse and be active (low) during the first centimeter on the graticule.

Connect the channel B scope probe to the read data test PCA test points for data channels zero through seven in turn. The pulse present at test points 0 through 6 should be the same as for test point P except that the channel zero pulse appears on the second centimeter of the graticule, the channel one pulse appears on the third centimeter, etc. The channel seven pulse should go low and remain low until the EOB pulse occurs.

Set the tape in reverse motion and check that the RC and EOB indicators on the read data test PCA are on, and the MTE, STE, and EVEN indicators are off.

The next section of the tape checks the ability of the error detection circuits to detect a skew buffer overflow, poisition the tape at the load point of section one. Use the CE switch on the control and status test PCA to set the tape in forward motion and, temporarily short the DRDY test point on the master PE read control PCA to ground. The STE and MTE indicators on the read data test PCA should light and the RC indicator should be off.

The next test checks the threshold detector, low amplitude detector and error detection circuits on the decoder PCA for each channel, the TIE decoder logic, and the single-track error and multiple-tract error circuits in the state control logic. These circuits should light the STE indicator when a single track error is simulated on any channel. Also, the MTE indicator is checked to see that it does not light erroneously under single-tract error conditions.

Position the tape at the load point of section one. Use the CF switch

on the control and status test PCA to set the tape in forward motion and temporarily short the DIFF test point, on the preamplifier PCA for channel P, to ground. The STE indicator on the read data test PCA should light and the MTE indicator should remain off (although it may flicker while the ground connection is made). Repeat this for clannels one through seven.

The next test verifies that the threshold detector, low amplitude detector, and error detection circuits on the decoder PCA for each channel and the TIE decoder logic and the MTE circuit in the state control logic are capable of detecting a low amplitude condition of the input signal on two channels from the preamplifiers. Also, the ability of the TIE decoder logic and MTE circuit to discriminate between a single-track error and a multiple-track error is checked. Position the tape at the load point of section one.

Short the DIFF test point on the P channel preamplifier to ground. Use the CF switch on the control and status test PCA to set the tape into forward motion and temporarily short the DIFF test point on the zero channel preamplifier to ground. The MTE indicator on the read PCA should be on only while both DIFF test points are grounded. Repeat this procedure for channels one through seven in turn (any two can be grounded at the sametime).

The next test checks that the error correction circuits generate an active EVEN signal when the required conditions exist. It also checks that the state control logic passes through all read-only states (00, 01, 03, 07, 17, 12, 02, 16, 13, and 11) while reading a data block. This is done by determining that the RC signal becomes active during the reading of each data block. Since the $\overline{RC}$ signal is initiated in state 02, $\overline{RC}$ signals occurring in two successive blocks indicate the state control logic has passed from state 00, through the data loop (status 17, 12, 02, and 16), through state 11 and back through state 02. Position the tape at the load point of section one.

Short the LSB test point for the P channel decoder PCA to ground

and use the CF switch on the control and status test PCA to set the tape into forward motion. The EVEN and MTE indicators on the read data test PCA should light.

Connect one oscilloscope probe to the RC test point on the read data test PCA. Connect the other oscilloscope probe to the DIFF test point on the P channel preamplifier and verify that two RC pulses occur for each block.

Remove the short on the P channel LSB test point and short, to ground, the LSB test point on the decoder PCA for each of channels zero through seven, in turn. For each channel, the EVEN and MTE indicators should light but only one RC pulse should occur per block.

The last test checks that the state control logic will detect an improper preamble while passing through states 00, 04, and 05 in read-after-write mode. Position the tape at the load point of section one.

Short the DIFF test point on the P channel preamplifier PCA to ground and set the tape into forward motion. The STE indicator on the read data test PCA should light. Now short the LWRITE test point on the data and status PCA to ground. The STE and MTE indicator on the read data test PCA should be on and the RC indicator off.

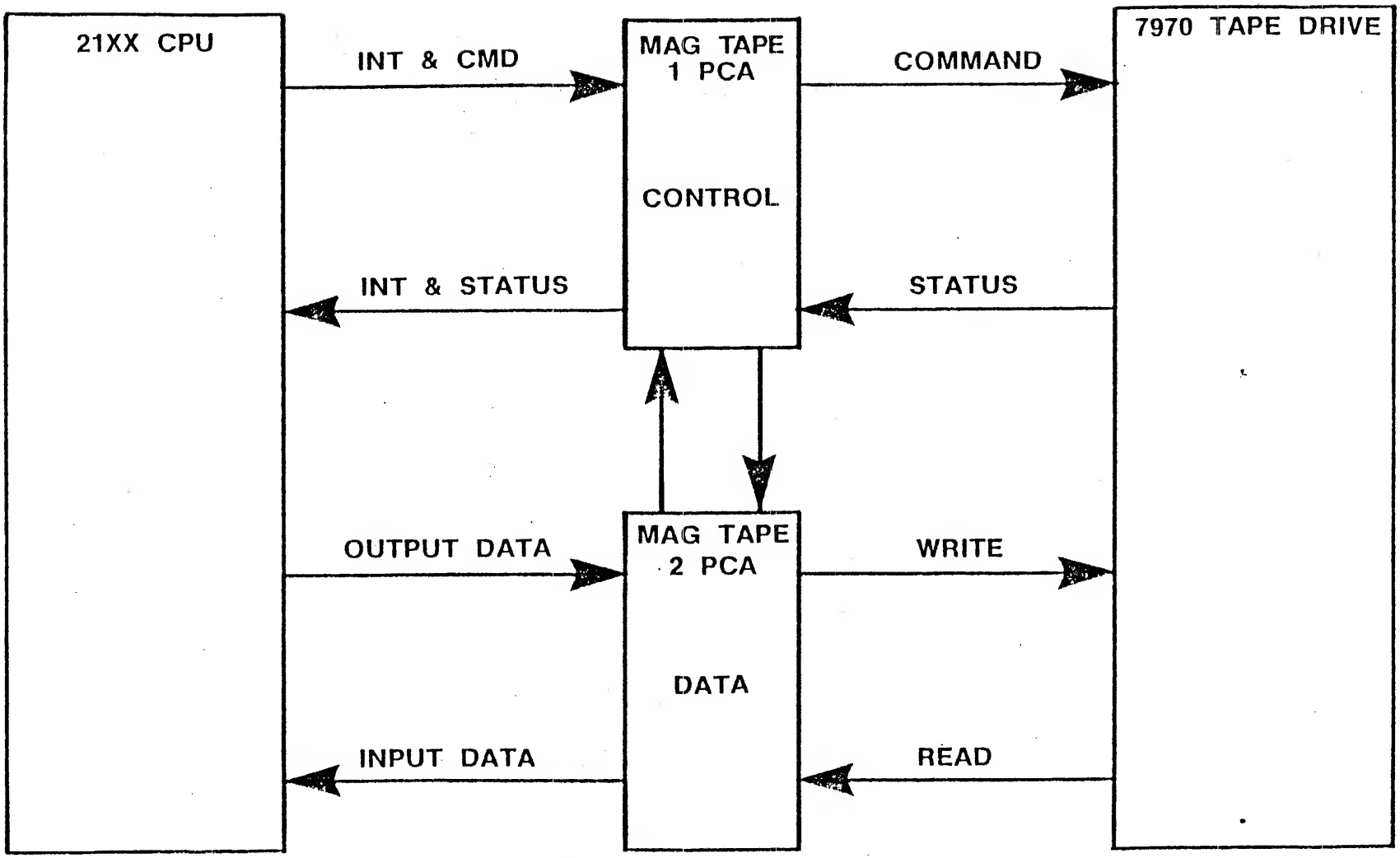
XI. Interfaces

A. 13181A Block Diagram

The 13181A interface provides the connecting link between 21XX CPU's and 7970B tape drive. The interface is comprised of two PCA's and one interconnect cable. The PCA's are Mag Tape 1 and Mag Tape 2 PCA's.

Mag Tape 1 PCA receives the interrupt and command signals from the CPU and generates the appropriate command signals to the tape drive. It also receives status signals from the tape drive and converts these to interrupt and status signal for the CPU.

Mag Tape 2 PCA routes the read/write data signals between the CPU and tape drive.



HP 13181A CONTROLLER

BRIEF DESCRIPTION OF HOW THE
13181A CONTROLLER OPERATES

1. COMPUTER INITIATES OPERATION WITH ISSUANCE OF AN STC.

2. AFTER TAPE HAS COME UP TO SPEED, AND IS PROPERLY POSITIONED, *DATA* IS WRITTEN TO OR READ FROM TAPE.

3. AT CONCLUSION OF THE OPERATION, THE TAPE ENTERS THE *IBG* AND STOPS. A FLAG BIT IS SET TO NOTIFY THE COMPUTER THAT THE OPERATION IS COMPLETE.

4. OTHER OPERATIONS NOT INVOLVING READING OR WRITING POSITION THE TAPE SO THAT READING OR WRITING WILL HAPPEN AT THE PROPER POINT ON TAPE.

13181A CONTROLLER FEATURES

1. AUTOMATIC UNPACKING OF 16-BIT WORDS INTO *TWO* 8-BIT BYTES TO BE WRITTEN ON TAPE.

2. AUTOMATIC PACKING OF *TWO* 8-BIT BYTES INTO *ONE* 16-BIT WORD WHEN READING FROM TAPE.

3. AUTOMATIC GENERATION AND CHECKING OF THE VERTICAL PARITY BIT AND THE LRCC.

4. AUTOMATIC GENERATIÓN (*NO CHECKING*) OF THE CRCC.

5. CAPABLE OF DRIVING UP TO FOUR MAG TAPE UNITS.

6. AUTOMATIC GENERATION (ON COMMAND) OF THE FILE MARK, AND AUTOMATIC DECODING OF FILE MARK WHEN READ.

MAG TAPE #1 PCA

1. MASTER CLOCK.
2. TIMING CIRCUITS.
3. INTERRUPT CIRCUITS FOR BOTH I/O CHANNELS
   A. DATA CHANNEL (HIGH PRIORITY)
   B. COMMAND CHANNEL (LOW PRIORITY)
4. TAPE UNIT SELECT LOGIC.
5. COMMAND OUTPUT BUFFER.
6. COMMAND DECODING CIRCUITS.
7. STATUS ENCODING CIRCUITS.

MAG TAPE #2 PCA

1. WRITE CIRCUITS:

   A. UNPACKING BUFFER (ONE WORD - TWO TAPE BYTES).
   B. CRCC GENERATING CIRCUITS AND REGISTER.
   C. VERTICAL PARITY GENERATOR.
   D. FILE MARK GENERATING CIRCUITS.
   E. WRITE TIMING CIRCUITS.

2. READ CIRCUITS:

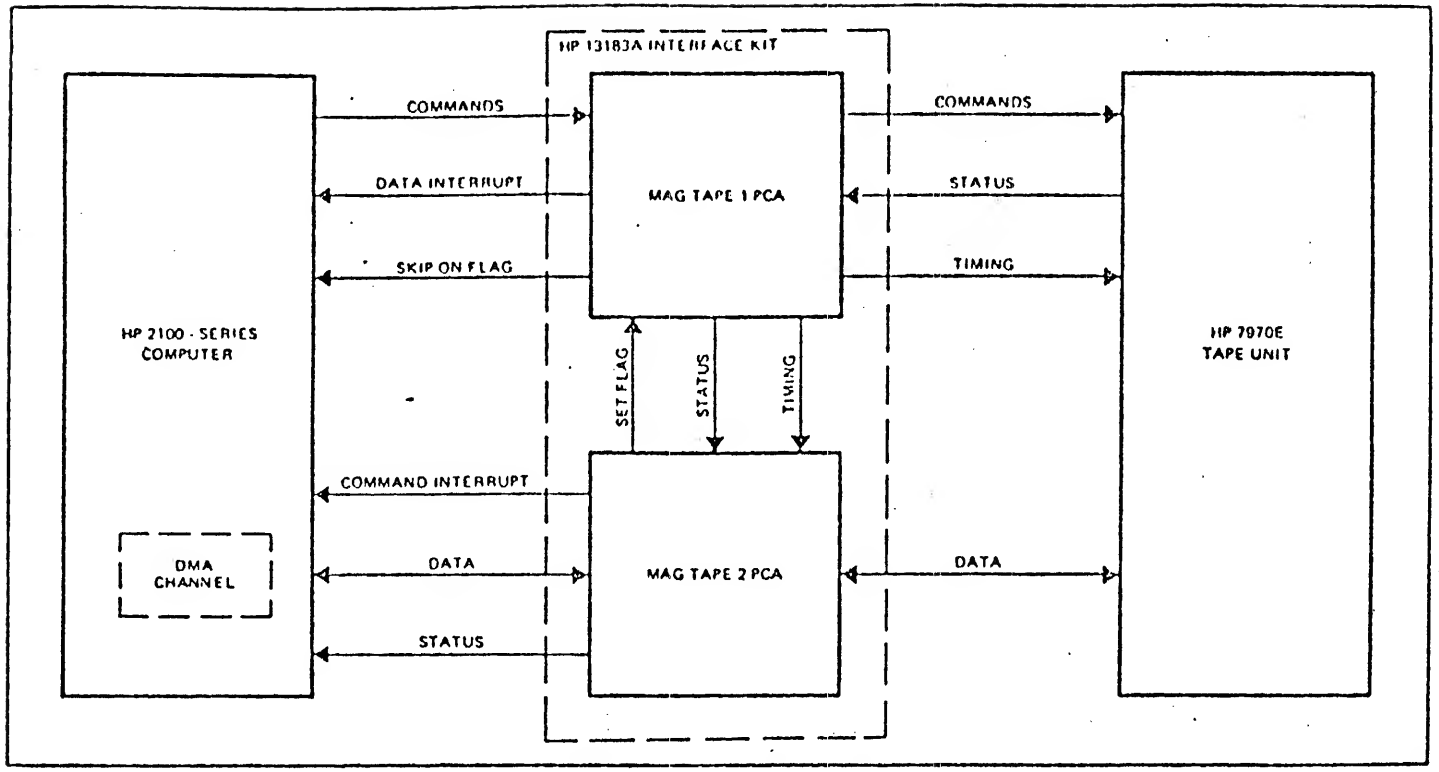
   A. VERTICAL PARITY CHECK.
   B. LRCC CHECK.
   C. FILE MARK RECOGNITION CIRCUIT.
   D. FILE SPACING CIRCUITS.
   E. PACKING BUFFER (TWO TAPE BYTES - ONE WORD).
   F. READ TIMING CIRCUITS.

B. 13183A Block Diagram

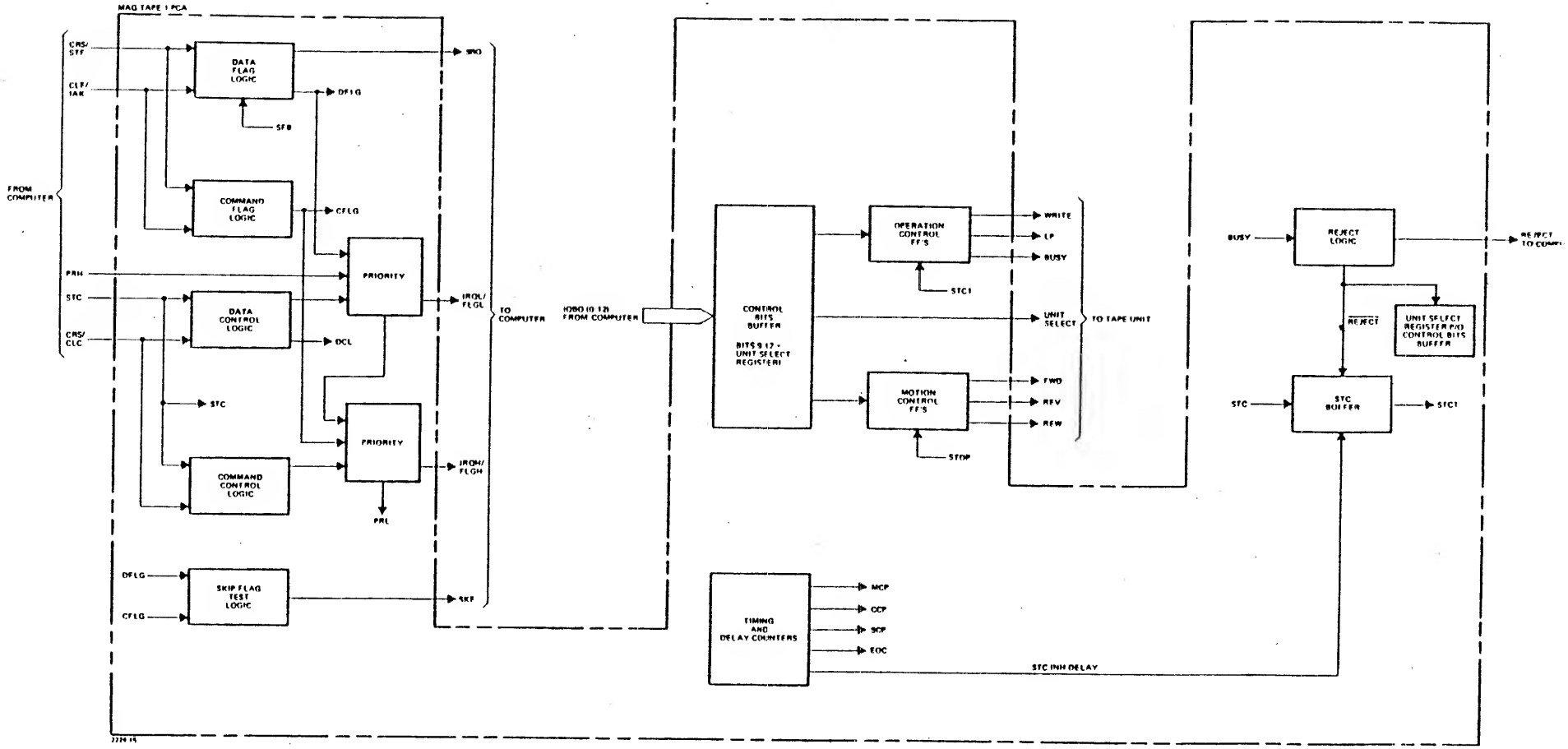
The 13183A is the interface between 21XX CPU's and 7970E tape drives. The interface consists of Mag Tape 1, Mag Tape 2 PCA's and one interconnect cable.

Mag Tape 1 PCA provides most of the control and timing for the interface and the tape drive. It receives and decodes tape commands from the CPU, and it provides status and time to the Mag Tape 2.

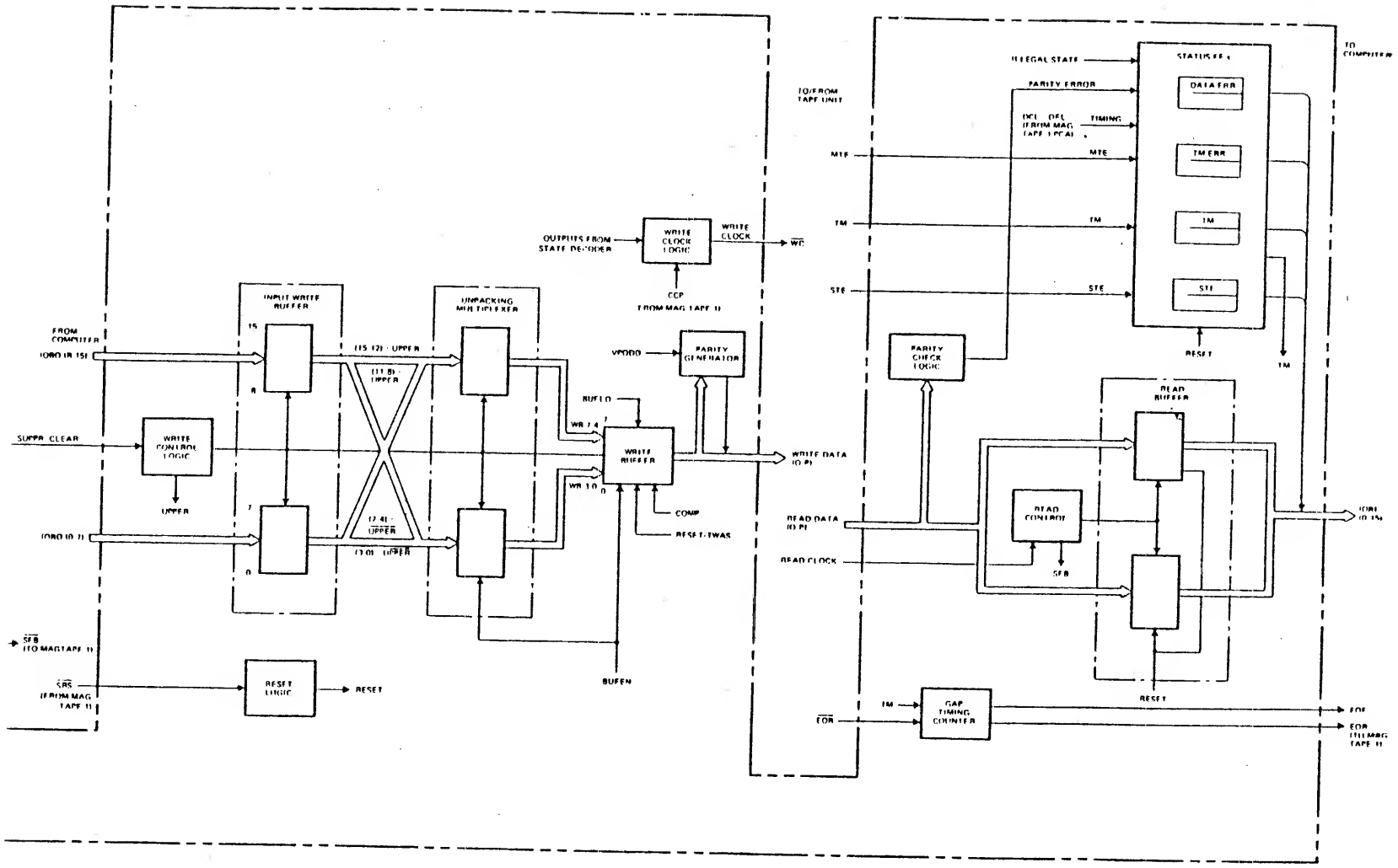
Mag Tape 2 PCA provides the data transfer path between the CPU and tape drive. During write operations, it unpacks 16-bit words from the CPU and transfers them to the tape drive as two 8-bit bytes. During read operations it packs data bytes from the tape drive into 16-bit words. These 16-bit words are transferred to the computer under control of Mag Tape 1.



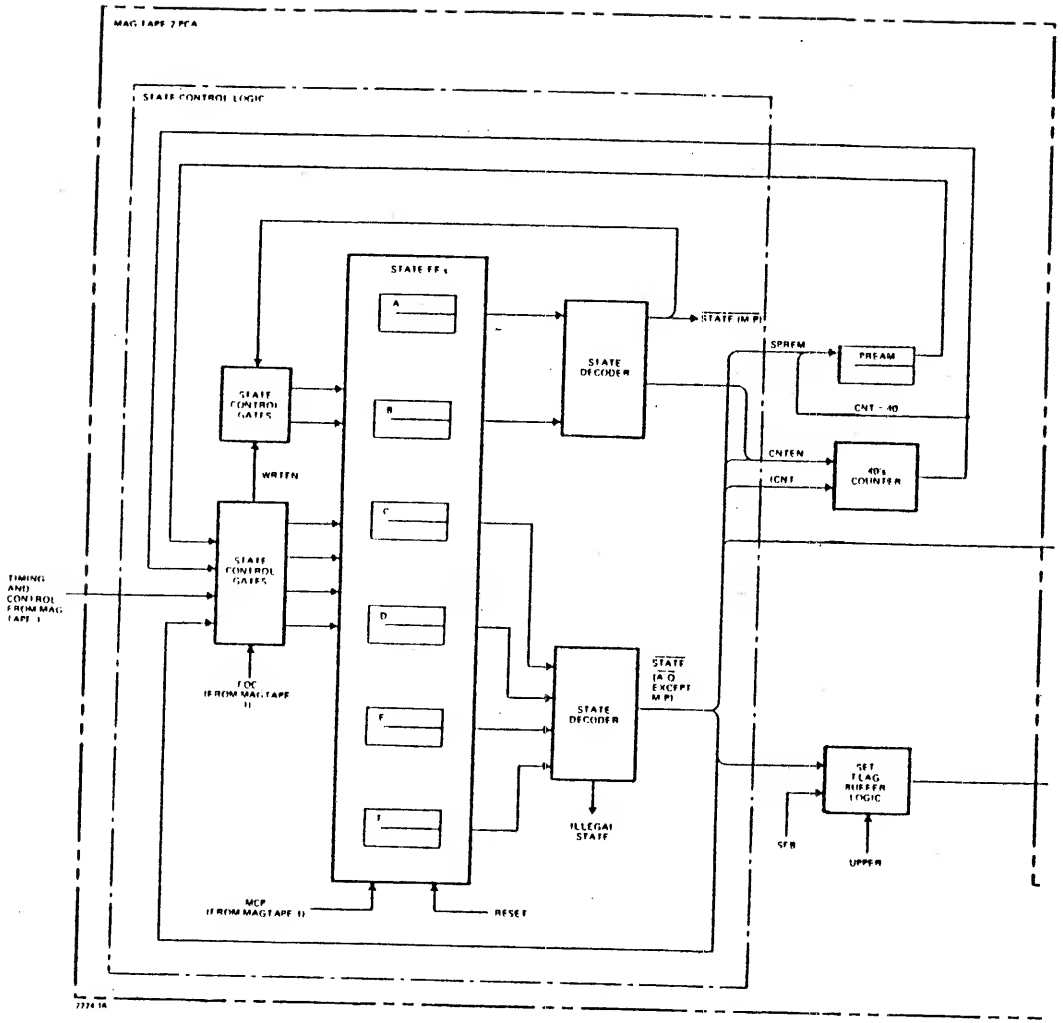
Interface Block Diagram



4-2. Mag Tape I PCA Block Diagra



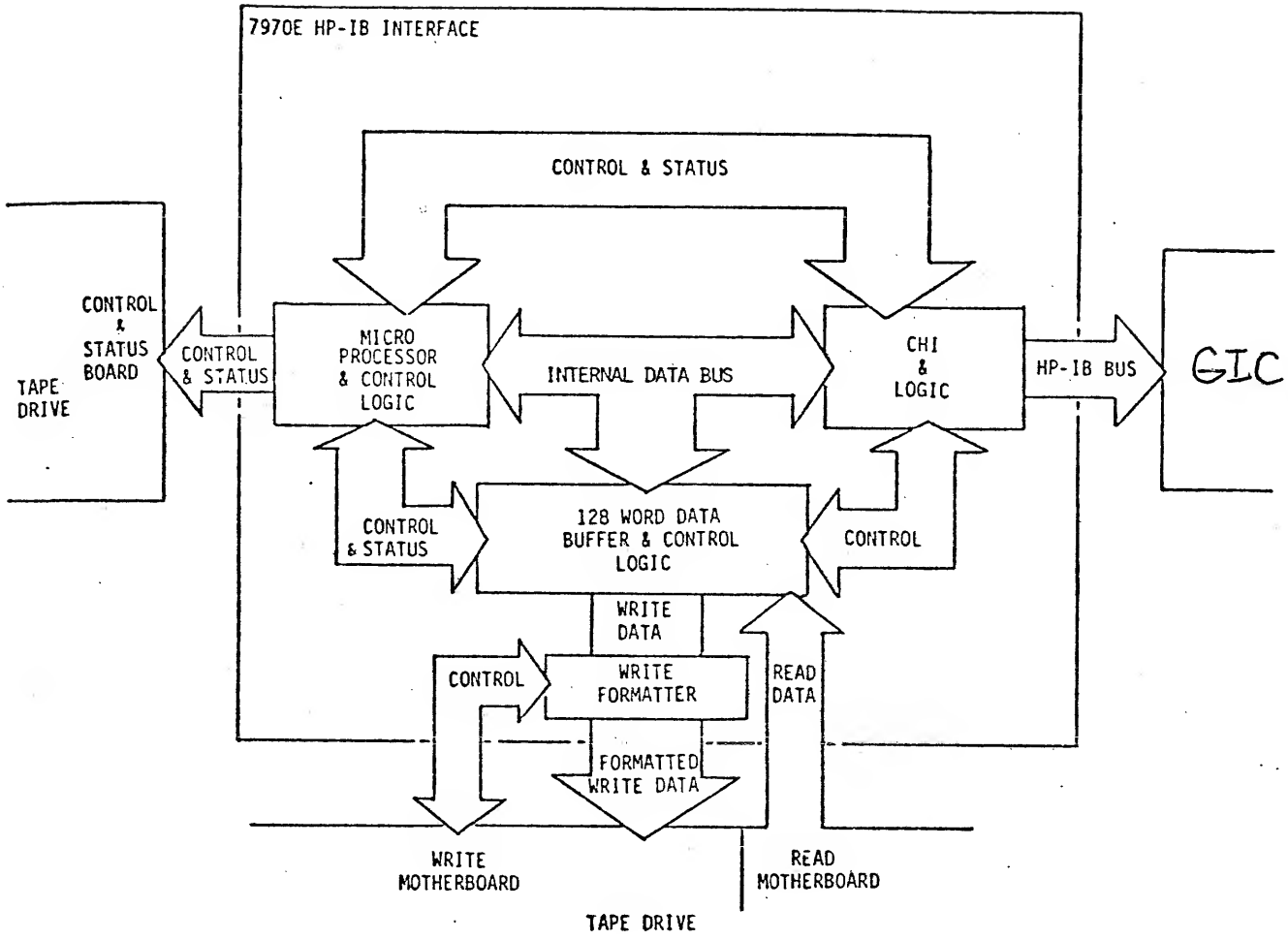
4-5. Mag Tape 2 PCA Block Diagram


MAG TAPE 2 PCA
STATE CONTROL LOGIC
STATE FF's
A
B
C
D
F
T
STATE DECODER
STATE (M P)
SPREM
PREAM
CNT = 40
STATE CONTROL GATES
WREN
CNTEN
ICNT
40's COUNTER
TIMING AND CONTROL FROM MAG TAPE 1
STATE CONTROL GATES
FOC (FROM MAG TAPE 1)
STATE DECODER
STATE (A O EXCEPT M P)
ILLEGAL STATE
SET FLAG BUFFER LOGIC
SFB
UPPER
MCP (FROM MAG TAPE 1)
RESET
7224 1A

C. HP-IB

The HP-IB interface provides the capability to connect a 7970E tape drive to a Hewlett-Packard interface bus system. It is a factory installed option only and is not available for field installation.

The HP-IB consists of a control PCA, write formatter PCA, back panel/switch PCA, and cables. For the 7970E tape drive to operate with the HP-IB, a modification to the read motherboard is required. The interface will not function if used with read control PCA's numbered 07970-62040. It uses a sixteen line bus comprised of these handshake lines, five control lines and eight data transfer lines.



7970E HP-IB INTERFACE BLOCK DIAGRAM

7970B ADJUSTMENT FOR READ/WRITE UNITS

VM 22 Capstan Motor Having Problems

TOOLS REQUIRED:

13191A	Control & Status Test Card
13192A	Write Test Card
HP 180A	Oscilloscope or equivalent
HP 3476A	Digital Voltmeter or equivalent
HP 5245L	Counter or equivalent
	Transport test tape HP P/N 5080-4525 or 5081-9401
	IBM master skew tape HP P/N 9162-0027
	Scratch tape

POWER SUPPLY CHECKS & ADJUSTMENT

+5, ±.05Vdc (adjust to 5, ±.01 Vdc when adjustment is required) BOISE +5V ± 0.1V

+12, ±.36 Vdc at +5V testpoint on Control & Status, Write and Read PCA.

-12, ±.36 Vdc

+5.00V +0.00 −0.05

NOTE Δ (reg & Bkplane) $\geq$ 0.7 volts there is a wiring problem.

Final reel servo adjustments must be made after the capstan servo adjustments. The capstan speed must be within tolerance in order to properly adjust the reel servo. However, tension must be maintained in order to make the capstan servo adjustments. If the tape unit does not maintain tension, perfrom the reel servo adjustments initially, complete the capstan servo adjustments, and repeat the reel servo adjustments.

Ck molex connectors at least once a year.

CAPSTAN MOTOR OFFSET CURRENT ADJUSTMENT

Prior to making the capstan motor offset current adjustment, verify the the power supply voltages have been adjusted. See figure 1 for location of switches and adjustment.

Connect a suitable dc voltmeter (capable of resolution to ±5 mv dc) across a 3-ohm resistor (R21 or R22) connected in series with the capstan motor. The common side of the resistance is associated with pin 2 or CJ1 and the high or motor side is associated with pin 2 of CJ2.

Load the tape transport and be sure tape is stopped. Adjust OFFSET control until voltmeter reading is minimum. An acceptable minimum is any value which is between +0.100 Vdc and -0.100 Vdc. Typical adjustment at room ambient temperature (25°C) will be in the order of ±0.080 Vdc.

CAPSTAN SERVO FORWARD AND REVERSE DRIVE SPEED ADJUSTMENTS (Counter required)

Connect counter to preamp Chan 3 for 9 track units

Chan 6 for 7 track units

Place unit in forward drive mode using FWD Switch (S2) on Capstan PCBA.
See figure 1 for location of switches.

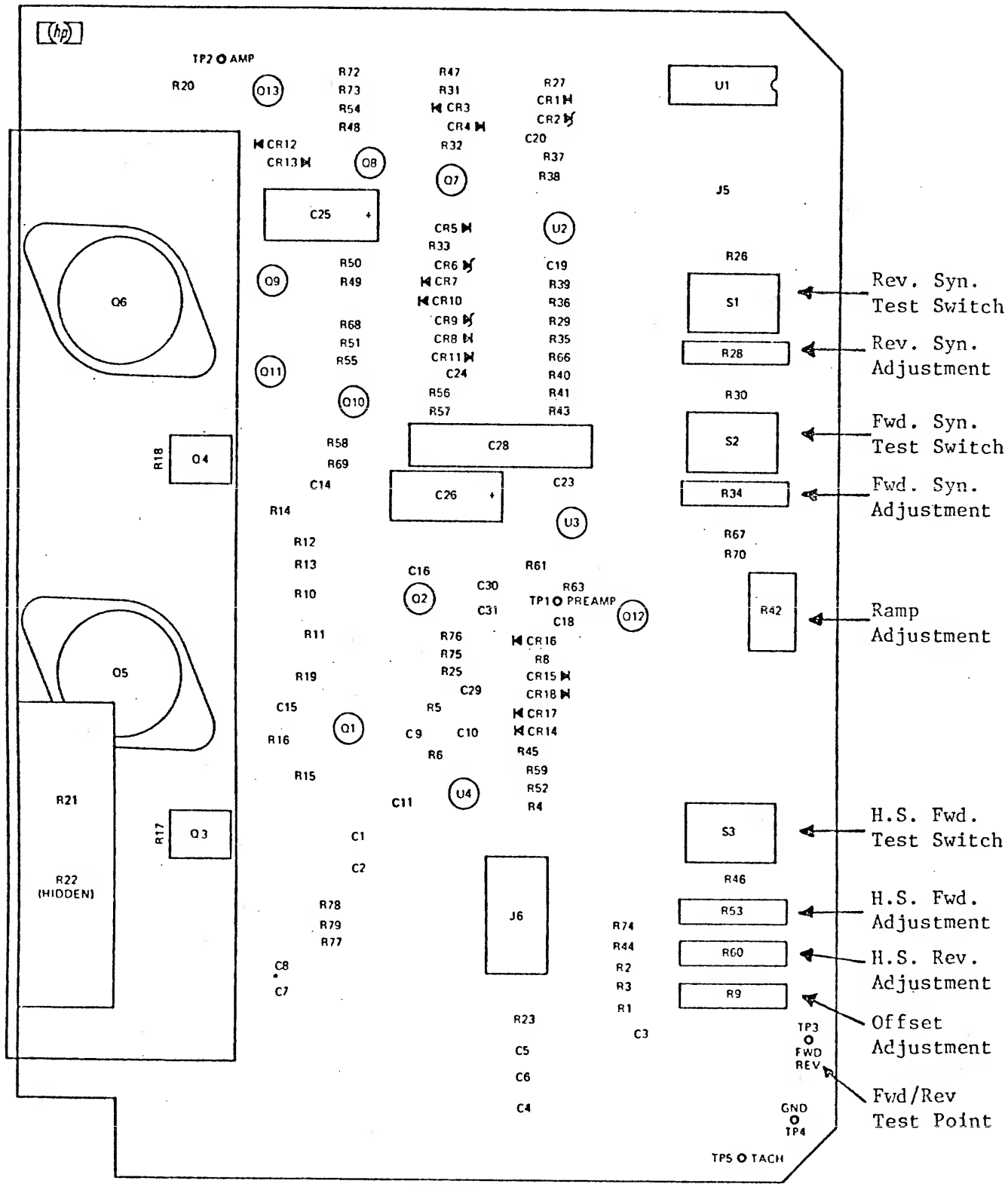


FIGURE 1

Adjust the FWD syn. control (R34) until counter reads as follows:

Start to Finish Δ ≤ 100 Hz

FOR:	45 ips	15 KHz, ±30 HZ
	37.5 ips	12.5 KHz, ±25 Hz
	25 ips	8,333 Hz, ±16 Hz

NO EXCURSIONS > 60Hz

Place unit in reverse drive mode using REV switch (S1) on Capstan PCBA.

Adjust the REV. Syn. Control (R28) until counter reads the same as forward speed.

HIGH SPEED REVERSE (Rewind)

Place unit in rewind mode by using the local rewind swtich on control panel. Adjust -160 (R60) on capstan PCBA for a counter reading of 53.333 KHz, ±100 Hz.

CAPSTAN SERVO RAMP SLOPE ADJUSTMENT

Operate the tape unit in a forward-stop-forward mode. The 13191A test card can be used. Place the MANUAL/PROGRAM switch in the PROGRAM mode. Place the FWD switch in the ON position.

Connect an oscilloscope to the FWD/REV test point on the capstan servo PC assembly. Sync the oscilloscope with the negative going edge of the forward command. (Test point 9 of the control and status PCA assembly or test point CF of the control and status test board.)

Adjust the capstan servo PC assembly RAMP control (see figure 1) to obtain the time listed in table 1 for tape unit synchronous speed. Use the vertical gain vernier control of the oscilloscope to expand the waveform so that the 90% point may be conveniently measured.

NOTE

On HP 180 oscilloscopes, the vertical spacing is a special horizontal time scale at 7.2 divisions which may be used to measure the time at the 90% level. See figure 2.

Table 1 Capstan Servo Start/Stop Time

SPEED (ips)	TIME (90%)	NOTE
25	12.6 ms	Tolerance for 90% time using the forward command is ±0.2 ms. Stop ramp time should be within ±0.5 ms of the applicable start ramp.
37.5	8.1 ms	
45	6.6 ms	

ck Tach Feedback >100 mv. in man mode.

REEL SERVO ADJUSTMENTS

Load a short length of tape onto the transport and bring to load point. The following adjustment determine the peak deflections of the tension arms. The amount of deflection desired is a function of the synchronous speed. At the highest speed (45 ips) the deflection is set so the tension arms deflect to the outer marks located on the back side of the casting, both in forward and reverse drive modes. At lower speeds the amount of deflection is smaller (i.e., at 25 ips the deflection is about half (25/45) the amount at 45 ips). Due to non-linearity of the tension arm transducer the swing of the tension arm may be unsymmetrical in the forward and reverse drive modes. (This will mean the tension arm will not be centered when there is not tape motion and is normal). With the supply reel loading with approximately 200 feet of tape, rotate the supply (lower) variable resistor counterclockwise for the proper deflection.

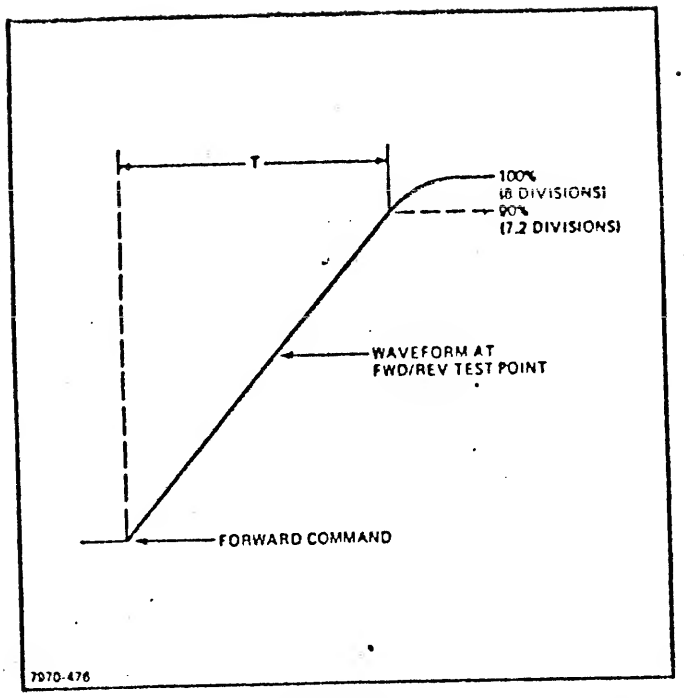


FIGURE 2

Stop tape motion and put in reverse drive and make sure the amount of deflection is the same in forward drive. If not, readjust the mask position until symmetrical swings of the proper amount are achieved. Repeat procedure for the take-up reel with approximately 200 feet of tape on the take-up reel.

PREAMPLIFIER GAIN ADJUST

Install 13191A Control & Status Test PCBA in unit. Place the MANUAL/PROGRAM slide switch in MANUAL position.

Install 13192A Write Test PCBA in unit. Place the BLOCK/CROSSTALK switch in CROSSTALK position.

On 13191A Control & Status Test PCBA, place the WSW switch in up position. Place the FWD switch in the up and down position. The tape unit should stop and LED on 13192A write test PCBA should be on.

Connect oscilloscope to the WC test point on write control PCBA. Adjust variable resistor on 13192A for the following bit to bit spacing:

FOR:	45 ips	111 µsec	NOTE
	37.5 ips	132 µsec	This will provide all "1's" at 200 ips.
	25 ips	200 µsec	

On the 13191A test PCBA, place the FWD switch in up position.

Using the oscilloscope, monitor TP's on preamplifier, adjust the preamplifier gains to 6.4 Vdc +.2, -.4.

FORWARD STATIC SKEW COMPENSATION ADJUSTMENTS

The techniques for rapid adjustment and for evaluating the need for adjustment differ. Figure 3 shows poor skew alignment and proper skew alignment. To adjust static skew componsation proceed as follows:

Load the master alignment tape, HP P/N 9162-0027, and place the tape unit in synchronous forward mode the adjustment operation.

Adjust the FWD skew delay control of channel 2 until resistor is approximately 1/4 turn from CCW position. Channel 2 will be reference channel for remaining adjustments.

Connect the oscilloscope channel A probe to the SKEW test point of the reference channel (2). Connect the oscilloscope channel B probe to each SKEW test point in succession and algebraically add oscilloscope channels A and B.

Adjust each channel skew delay variable resistor for a maximum displayed amplitude.

REVERSE STATIC SKEW COMPENSATION ADJUSTMENTS

Reverse static skew compensation is accomplished in exactly the same manner as that used for forward skew except for the use of reverse drive mode and adjustment of reverse skew controls. The same SKEW test points are used for both adjustments.

READ CHARACTER GATE ADJUSTMENTS

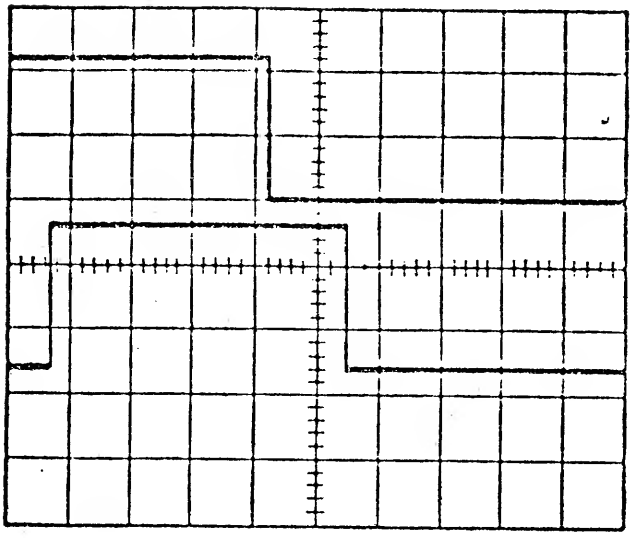
Load the tape unit with the master alignment tape, HP P/N 9162-0027, place the unit in synchronous forward operation, and select 800 ips operation (seven-track units only).

Synchronize the oscilloscope (negative slope) to the NOR test point on the read control card. (The first data bit of a character will start the gate tiem when this line goes to ground.)

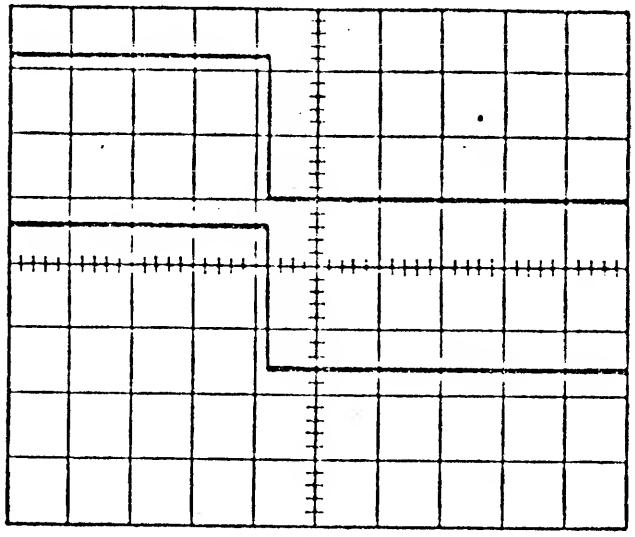
Observe the bit-to-bit time (negative-going edge to negative-going edge). The low (or ground) portion of this signal represents the character gate time.

Adjust R29 on the read control PCBA so that negative portion of square, wave represents 46% of the bit-to-bit time. In actual time it can be adjusted for the following times:

45 ips	12 to 13 usec
37.5 ips	15 to 16 usec
25 ips	22 to 23 usec

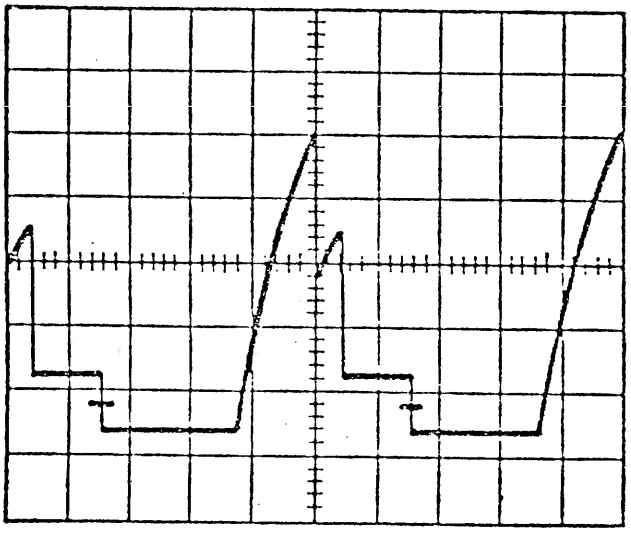


POOR SKEW ALIGNMENT

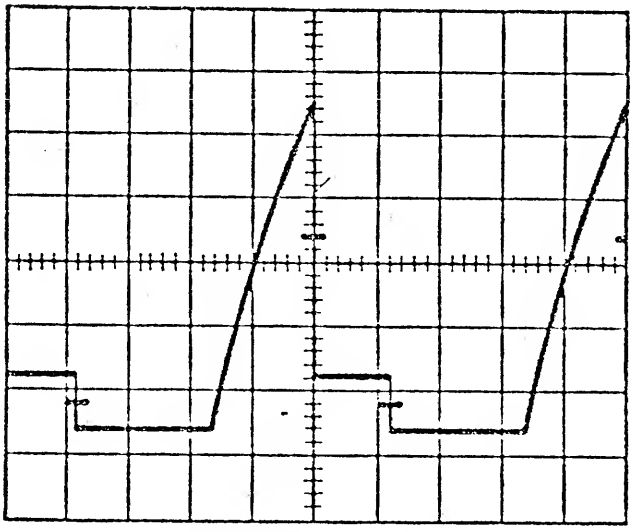


GOOD SKEW ALIGNMENT

New Read PCA



POOR SKEW ALIGNMENT



GOOD SKEW ALIGNMENT

Old Read PCA

7970-528

FIGURE 3

WRITE ADJUSTMENT PROCEDURES

Load the tape transport with a reel of scratch tape equipped with a write enable ring. Place the unit in synchronous forward write mode and write a data pattern consisting of all "ones", at 800 cpi.

NOTE

To obtain 800 bpi all 1's, use the procedure outline in PREAMP ADJUSTMENTS. However, this time set the bit-to-bit spacing as follows:

FOR:	45	ips	27.9 usec
	37.5	ips	33 usec
	25	ips	50 usec

Adjust the write skew delays as follows:

Adjust the channel 2 write skew delay until channel 2 resistor is approximately 1/4 turn from CCW position. Channel 2 will be used as a reference channel.

Connect the oscilloscope channel A probe to tape unit channel 2 read SKEW test point, and connect the oscilloscope channel B probe to the SKEW test point corresponding to the write data channel being adjusted. Set the oscilloscope controls to algebraically sum channels A and B. Adjust oscilloscope sweep to display at least one full bit time (leading edge of one bit to the leading edge of the next).

Adjust the skew delay variable resistor of the channel under adjustment to obtain a maximum amplitude on the oscilloscope display.

Repeat step "c" for all remaining channels except the reference channel (channel 2).

NOTE

Under no circumstances are any of the read skew adjustments to be changed during the write skew compensation process.

7970E ADJUSTMENT FOR READ/WRITE UNITS

TOOL REQUIREMENT:

13191A	Control and status test card
13195A	Write formatter PCA
13196A, Opt 1	PE write test PCA
HP 180A	Oscilloscope or equivalent
HP 3476A	Digital voltmeter or equivalent
HP 5246L	Counter or equivalent
	HP P/N 5080-4525 (2400 feet)
	HP P/N 5081-9401 (1200 feet)
	NOTE: 7 track works both for 7/9 track drives
	IBM master skew tape, HP P/N 9162-0027
	Scratch tape

PREALIGNMENT

CLEAN HEAD AND TAPE GUIDES. Install the 13191A (Fig. 1) vertically into the upper left of the control and status board and set all switches down, including the PROG/MAN slide switch. Install the 13195A (Fig. 3) horizontally above the write card cage. Make sure that the jumper U23 is correctly placed to match the speed of the machine (Fig. 4), and the parity jumper goes to Pin 3. Install the 13196A option 1 (Fig. 2) vertically into the 13195A board and set all switches to the left. Place the 2 switches on the capstan servo PCA down. This will be the reset position of all the switches. Be sure all +5V are connected.

POWER SUPPLY CHECKS AND ADJUSTMENT

+5V — Adjust port on power regulator board to obtain +5 Vdc (±0.01 Vdc) on the +5 Vdc test point of the power regulator card.

+12V — Verify +12 Vdc (±0.36 Vdc) on the +12 Vdc test point of the power regulator card.

-12V — Verify -12 Vdc (±0.36 Vdc) on the -12 Vdc test point of the power regulator card.

NOTE: Reel servo adjustment may have to be adjusted here to maintain tension, however, it must also be checked in the order in which it appears in this alignment procedure.

CAPSTAN MOTOR OFFSET CURRENT ADJUSTMENT

Connect a suitable dc voltmeter (capable of ±5 mVdc resolution) across one of the two 3 ohm resistors (Fig. 5, R21 or R22). The common side is to pin 2 of CJ1 and the high motor side is to pin 2 of CJ2. Load transport test tape (speed tape) to the BOT tab. Adjust offset (Fig. 5, R9) such that voltage across resistor is 0.0 Vdc (±0.09 Vdc).

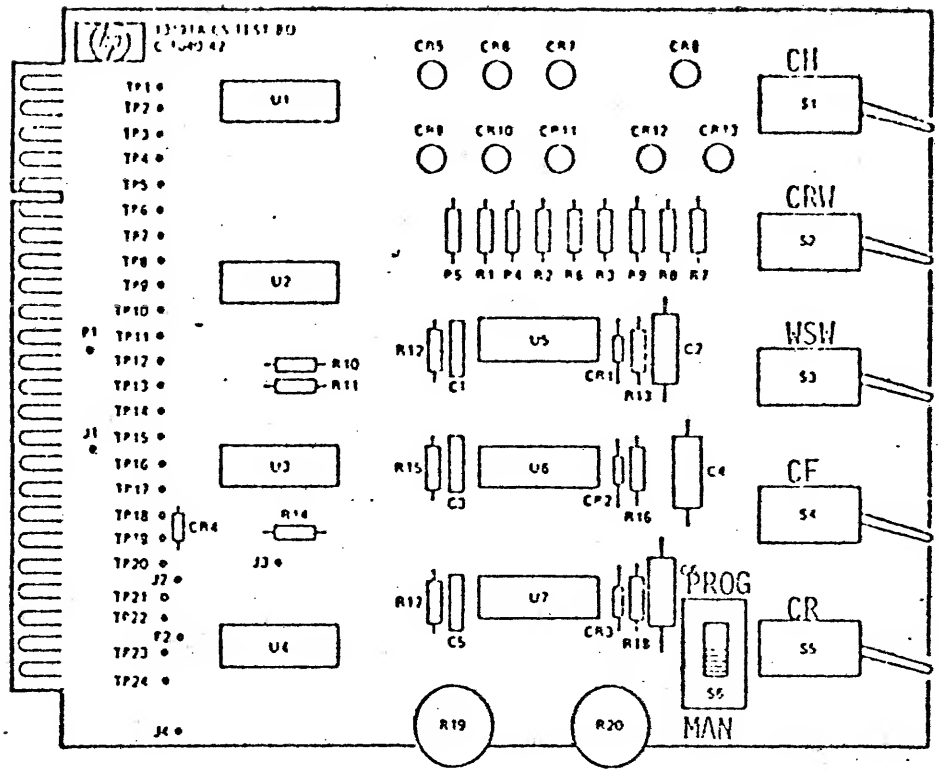


Figure 1. CONTROL AND STATUS TEST BOARD

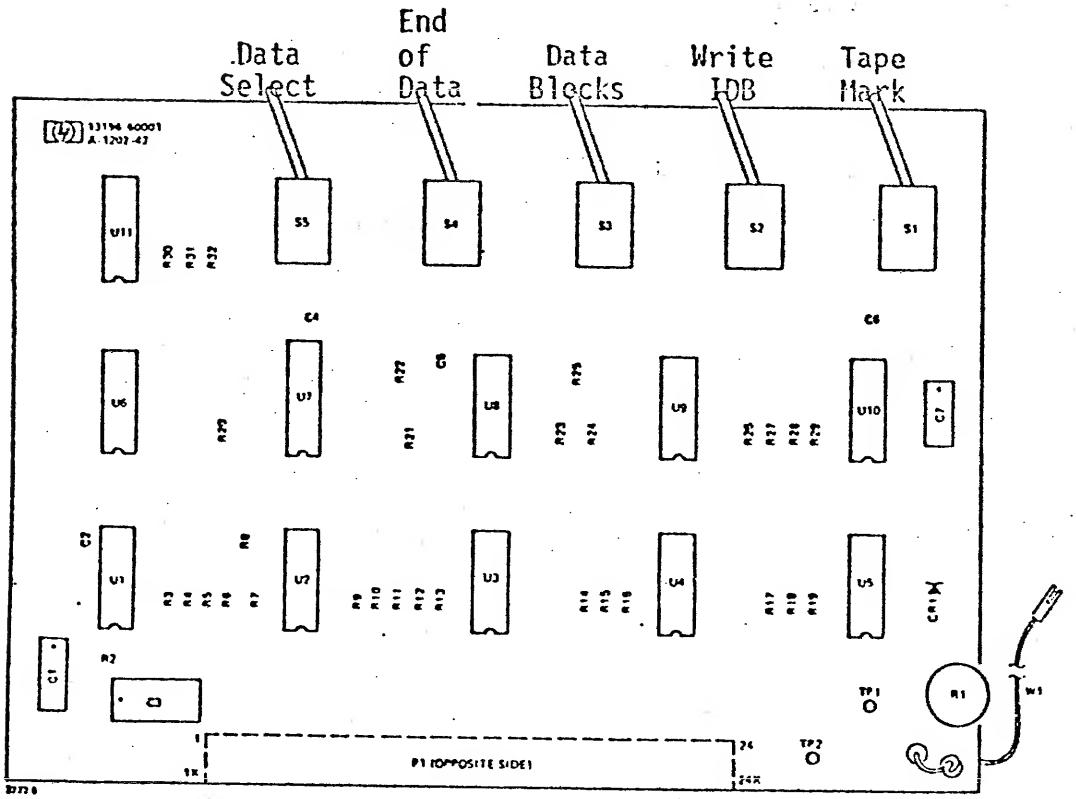


Figure 2. PE TEST CARD

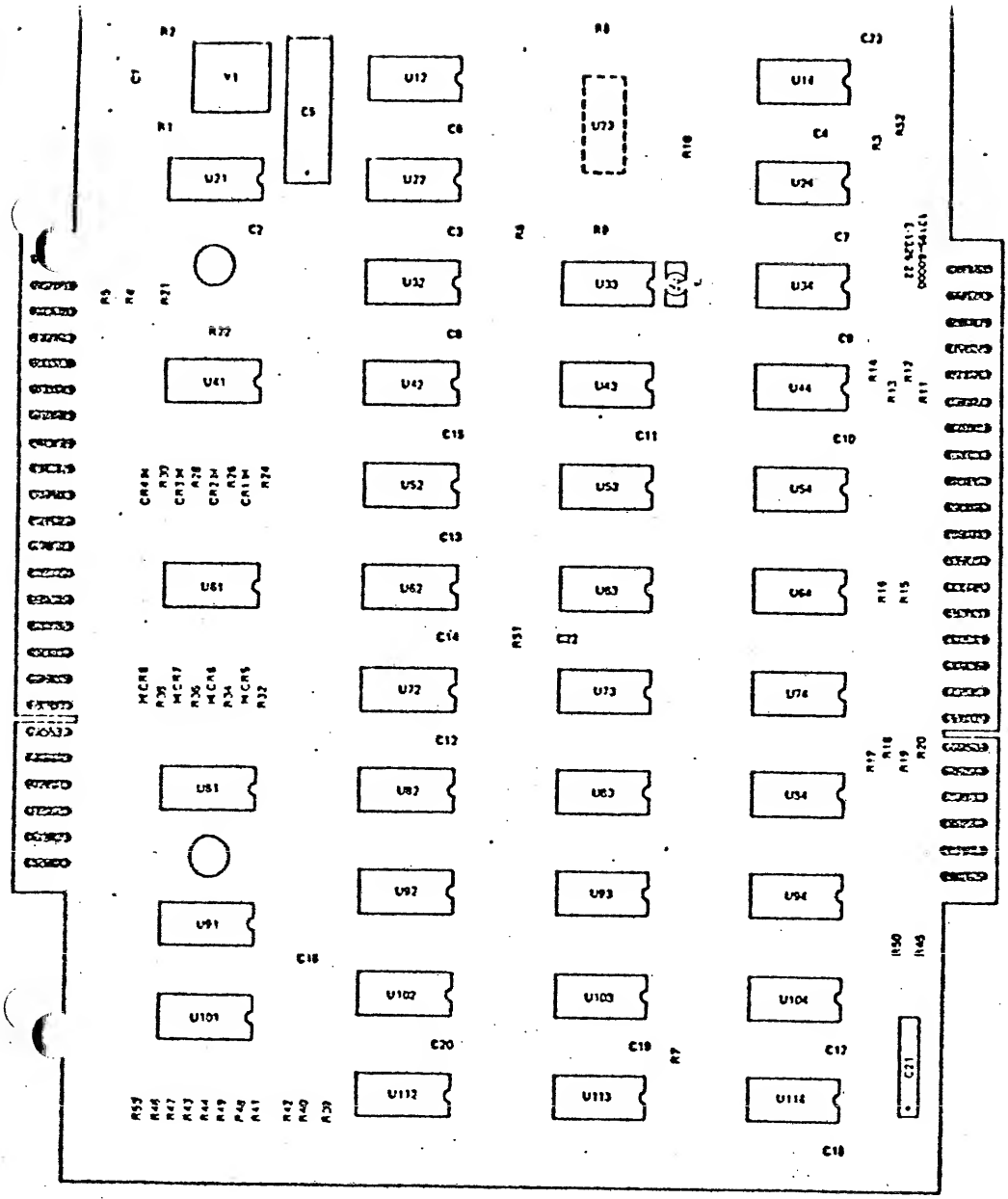


Figure 3. 13195A

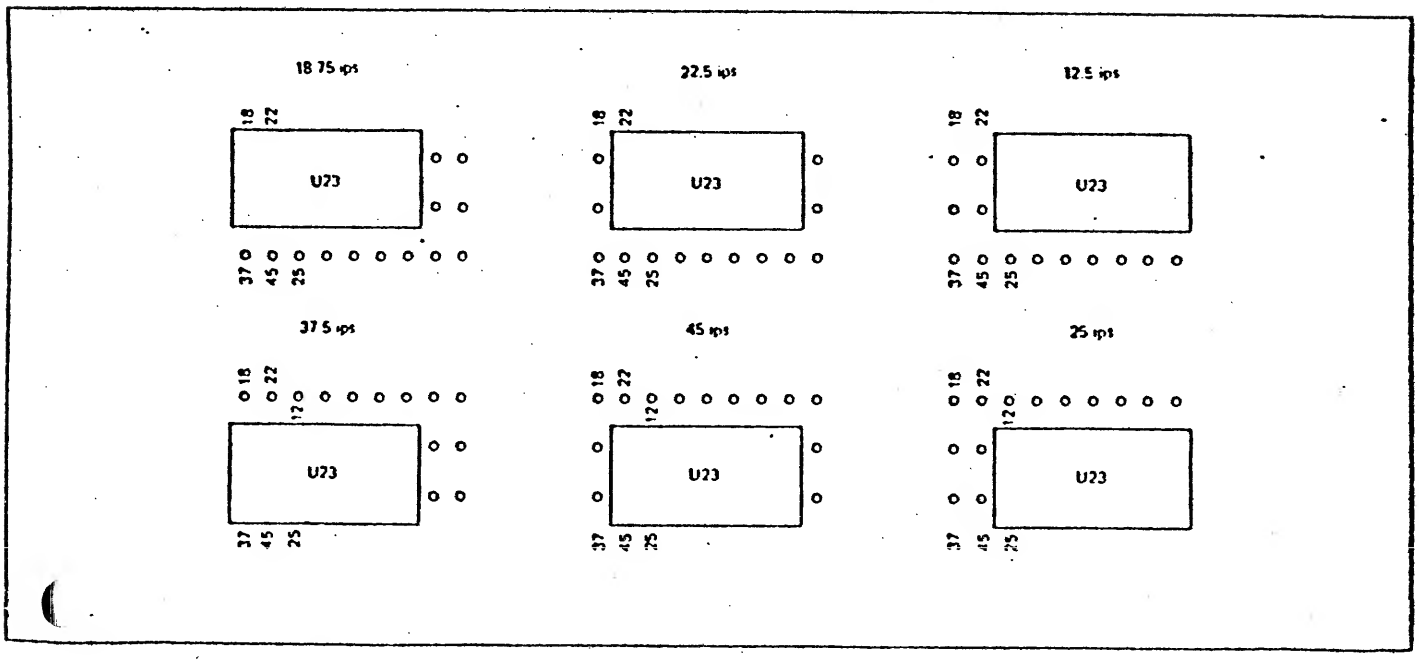


Figure 4. U23 JUMPER POSITION

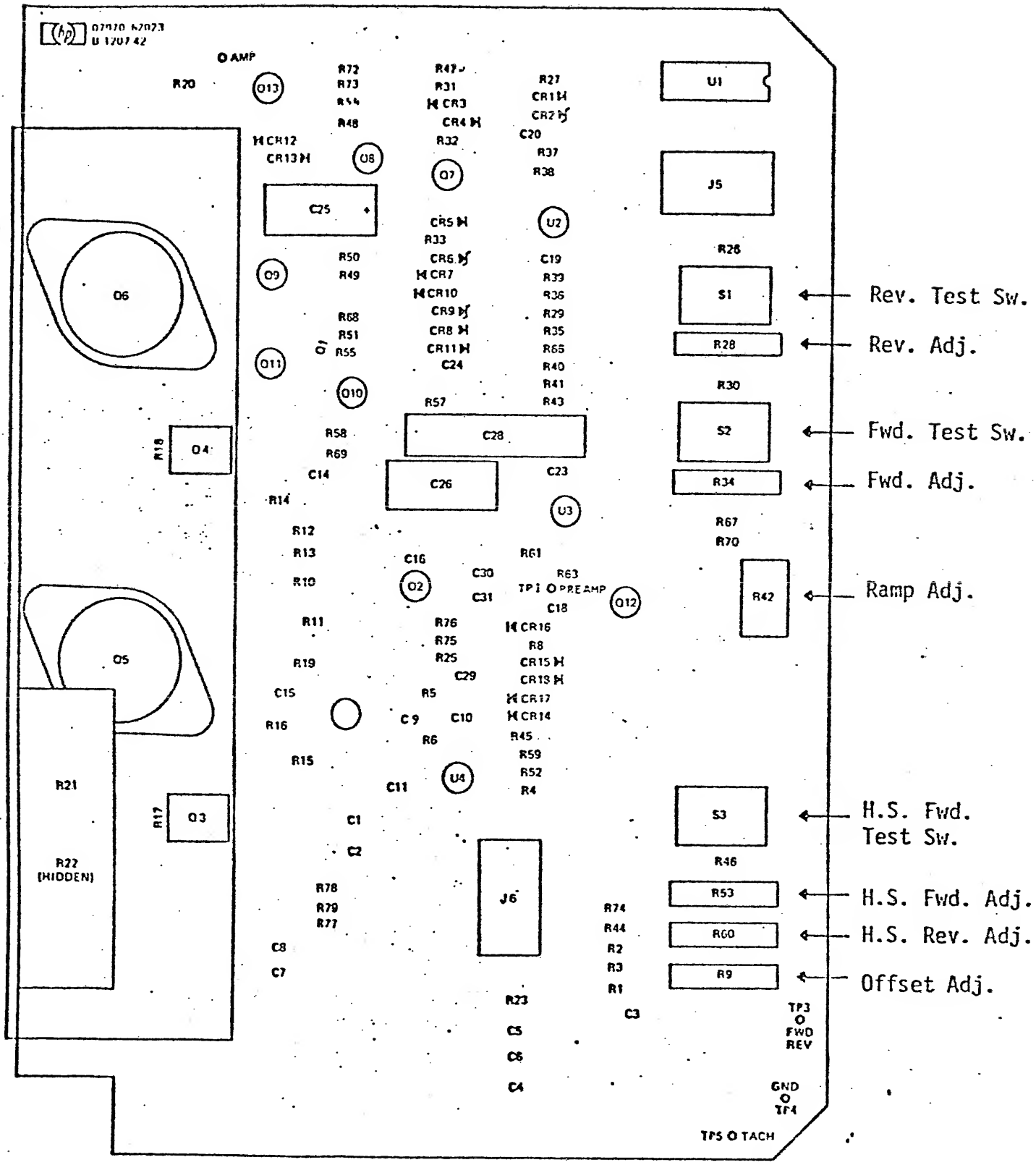


Figure 5. CAPSTAN SERVO PCBA

TENSION ARM AND REEL SERVO ADJUSTMENT

Load a short length of scratch tape on the transport and bring the tape to load position. Have approximately 200 feet or tape on the supply reel, proceed to adjust the supply renstion arm. If the deflection of the tension arm is not centered between the limit switches during forward and reverse movement, lightly loosen the allen screw in the center of the tension arm and slowly turn the mask in the appropriate direction. While holding the tension arm girm, tighten the allew screw. Besure that the mask does not rub on the tension arm hood. The peak deflection of the arm should also be adjusted by R106 on the reel servo amp shown in Figure 6, below. On a 45 ips machine, the swing should come approximately 1/4 inch from the limit switches. If this is not possible, make sure the filament in the tension arm lamp is parallel to the mask. If you still cannot get proper deflection, check the tension arm assembly for slower machines, the arm swing is proportionate to the speed. (Example, a 25 ips machine should swing 25/45 of a 45 ips machine.) Now have 200 feet of tape on the take-up reel and repeat the above using the take-up mask and R104 of Fiture 6.

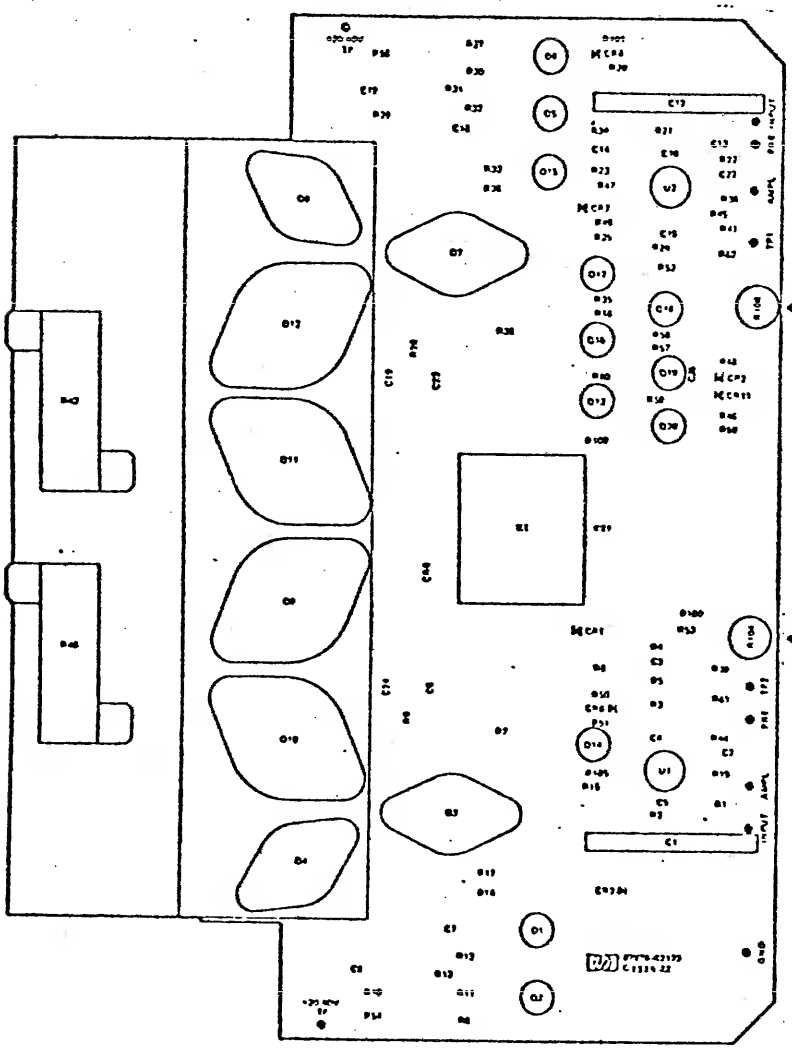


FIGURE 6.
REEL SERVO PCA

CAPSTAN SERVO FORWARD/REVERSE/REWIND DRIVE SPEED ADJUSTMENTS

There are two test points available for each preamp. Use the ones marked "DIFF". Connect counter to preamp channel 3 test point for 9 track or preamp channel 6 test point for 7 track. Place drive in forward mode using forward test switch (Fig. 5, S2). Speed versus frequency is given in the chart below:

45	15	kHz ±30Hz
37.5 ips	12.5	kHz ±25Hz
25 ips	8.33	kHz ±16Hz

Adjust forward pot (Fig. 5, R34) to obtain the above specifications. Place S2 off and S1 (Fig. 5, Reverse Test Switch) up and adjust reverse pot (Fig. 5, R28). Place S1 off and S3 (Fig. 5, High Speed Forward) on. Adjust high speed forward (Fig. 5, R53) to 53.33 kHz (±100 Hz). Place S3 off and push the front panel rewind push button, adjust high speed reverse (Fig. 4, R60) to obtain 53.33 kHz (±100 Hz). Reset switches.

CAPSTAN SERVO RAMP SLOPE ADJUSTMENT

Place the PROG/MAN switch (Fig. 1, S6) in the PROG position and the CF switch (Fig. 1, S4) up. Connect channel A to the forward/reverse test point (Fig. 5, TP3). Sync the scope on the negative edge of the oykaw ub TP9 of the control and status PCA. Adjust the ramp pot (Fig. 5, R42) such that 90% of the rise time of the ramp is within the following specifications:

45	ips	6.6 ±0.2mS
37.5	ips	8.1 ±0.2mS
25	ips	12.6 ±0.2mS

See Figure 8 for illustration. The stop ramp should be varified to be within 0.5 mS of the start ramp. This can be done by changing the polarity of the scope syce from negative to positive. Reset switches when ramp slope adjusted.

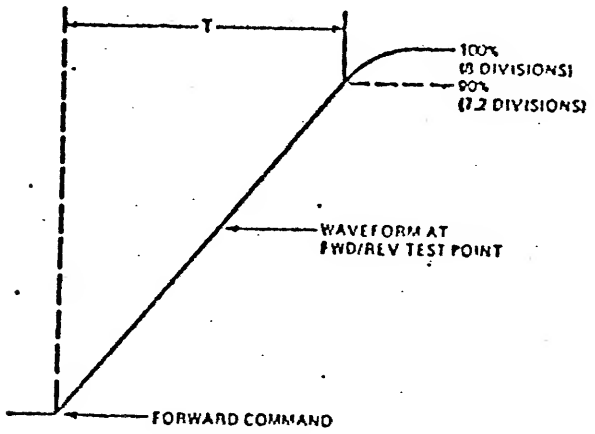


FIGURE 8. RAMP ILLUSTRATION (REVERSE RAMP IS MIRROR IMAGE).

PREAMP GAIN ADJUSTMENT

Place the WSW switch up and the CF switch up (Fig. 1). Place the DATA SELECT and WRITE DATE BLOCKS switches in the right position. (The tape drive should now be writing in all channels.) Monitor the DIFF test points on the preamp and adjust the gains to 4.5 volts ($\pm$0.3V) with the pots directly to the rear of the test points. Reset switches.

WRITE SKEW DELAY

Mount a master skew tape. Place the CF switch up, determine the amount of skew in each of the read decoder cards by placing probe "A" on the DAT test point of the read decoder card channel 2 (4th card over from left in read card cage), and probe "B" sequentially on the other 8 DAT test points. Set the scope to A chop B. The amount of skew to be recorded is the distance in mS from the trailing edge of channel 2 to the trailing edge of the other channel being measured. It may be plus or minus. See Figure 7 below. After the amount of read head static skew is noted, remove the master skew tape and mount a scratch tape with a write enable ring. Place the WSW and CF switches up. Place the DATA SELECT and WRITE DATA BLOCKS to the right. Set the channel 2 write skew adjustment 1/4 of the way from the full counterclockwise position. Place channel "A" of the scope on channel 2 of the write card cage and sequentially monitor the other 8 channels with probe "A". Set the trailing edges to reflect the same amount of skew as noted while reading the master skew tape for each individual channel.

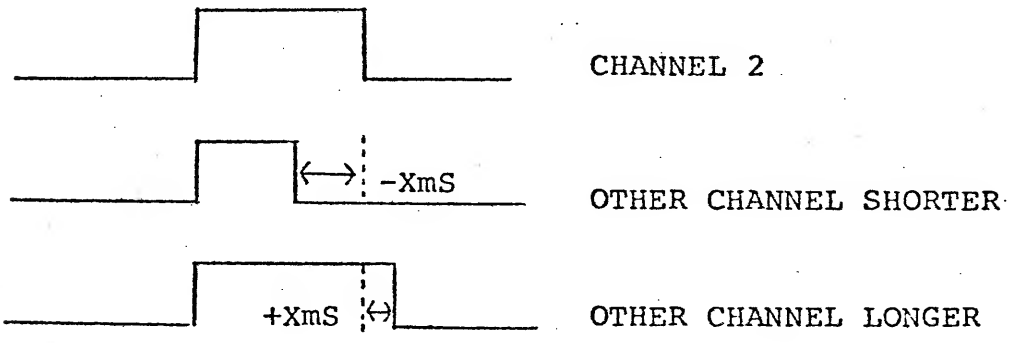


FIGURE 7

BOT/EOT ADJUST

The BOT/EOT test points are located on the bottom of the control switch assembly. Put the drive on a BOT tab and measure the BOT test point. If the voltage is less than 1.0 vots, make sure the filament in the lamp is perpendicular to the transport. If the voltage is still less than 1.0 volt, change the photosence lamp. Manually rotate the capstan pulley until the load point tab is no longer under the photosence assembly. The voltage should now measure -.4V. Performs the same measurements for the EOT tab.

INTER-OFFICE SERVICE MEMO

TO: "MAILS"

FROM: Boise Division Product Support

SUBJECT: 7970A/B/C/E ASSEMBLY PART NUMBERS AND EXCHANGE PART NUMBERS .

The standard configuration of the 7970A/B/C/E tape units contain many assemblies which are common. The following is a list of assemblies which are used in the 7970A/B/C/E. This list includes the original new part number, the exchange part number if one has been assigned, current replacement part number and parts usage by tape unit model number.

NOTE

The current replacement part number is for the new assembly. Consult that part number to determine if the current part number has an exchange part number assigned. For example, 07970-61060 new part number - exchange part number is 07970-61061; however, the current replacement part number is 07970-62173. Looking up 07970-62173, the exchange part number for it is 07970-62244.

BG:jmq

(Continued)

8-78/46

HP PART NUMBER 07970-	ASSEMBLY DESCRIPTION	7970A SPEED				7970B SPEED			7970C SPEED			7970E SPEED			EK. PART NUMBER 07970-	REPLACEMENT PART NO. 07970-	COMMENTS
		10-20.9	21-37.5	10-25	25.1-37.5	10-20.9	21-45	ALL	10-20.9	21-45	ALL	10-20.9	21-45	ALL			
60020	Power Regulator			X											N/A		
60030	Reel Servo			X											60031		
60040	Capstan Servo			X											60041		
60070	Photo Sense Assy.	X	X												N/A	62131	
60080	Control Switch Assy.	X	X												N/A	62089	
60090	Density Select Assy.	X	X					X							N/A		
60100	Unit Select Assy.	X	X												N/A	62086	
60110	Power Distribution			X											N/A		
60140	Capstan Motor	X	X			X						X			N/A		
60141	Capstan Motor							X						X	N/A		
60150	Write Enable Assy.	X	X												N/A	62122	
60230	Write Mother Bd. Assy.	X	X												N/A		
60240	Write Control	X	X					X						X	N/A		
60300	Write Interconnect	X	X				X								N/A		
60390	Read Mother Bd	X	X					X							N/A		
60400	Control & Status			X											60401		
60481	Tension Arm Assy.	X	X					X						X	N/A		
60500	Read Pre Amp	X													60501		Note 3.
60510	Read Pre Amp		X												60511	62000	
60520	Dual Chan. Read	X				X									N/A	62166	Note 1.
60530	Dual Chan. Read		X				X								N/A	62168	
60540	Read Control	X													N/A	62170	
60550	Read Control		X												N/A	62171	
60560	Single Chan. Read	X				X									N/A	62167	Note 1.
60570	Single Chan. Read		X				X								N/A	62169	

HP PART NUMBER 07970-	ASSEMBLY DESCRIPTION	7970A SPEED				7970B SPEED			7970C SPEED			7970E SPEED			EX. PART NUMBER 07970-	REPLACEMENT PART NO. 07970-	COMMENTS
		10-20.9	21-37.5	10-25	25.1-37.5	10-20.9	21-45	ALL	10-20.9	21-45	ALL	10-20.9	21-45	ALL			
61150	Photo Sense Assy.							X						X	N/A	62131	
62000	Read Pre Amp		X				X								62119		
62001	Read-Read Pre Amp					X									N/A		
62002	Read-Read Pre Amp					X									N/A	62001	
62003	Read-Read Mother Bd.	X	X					X							N/A		
62004	Read-Read Control	X				X									N/A		
62005	Read-Read Control		X				X								N/A		
62006	Density Select Assy R/R							X							N/A	62032	
62012	Read-Read Pre Amp						X								N/A		
62022	Write Enable Assy.							X						X	N/A	62122	
62023	Capstan Servo PCA				X			X						X	62084	62172	
62024	Reel Servo PCA				X			X						X	62085	62173	
62027	Capstan Servo Dual Speed													X	N/A		
62028	Head Assy/ R/W 9tr 21-45 IPS												X		N/A	62212	
62029	Head Assy. R/R/R 21-45 IPS												X		N/A	62214	Note 5.
62030	Head Assy. R/R 9tr 21-45 IPS												X		N/A	62201	
62031	Head Assy. R/W 9tr 10-20.9 IPS					X									N/A	62211	
62032	Head Assy. R/R/R 10-20.9 IPS											X			N/A	62213	
62033	Head Assy. R/O 10-20.9 IPS											X			N/A	62209	
62034	P.E. Pre Amp 21-45 IPS												X		62124		
62035	P.E. Pre Amp R/R/R 21-45 IPS												X		62135		Note 5
62036	P.E. Pre Amp 10-20.9											X			N/A		
62037	Slave P.E. Read Assy													X	62125		
62040	P.E. Read Mother Bd.													X	N/A		
62041	P.E. Decoder													X	62126	~~62294~~ 62353	

PART NUMBER 7970-	ASSEMBLY DESCRIPTION	7970A SPEED				7970B SPEED			7970C SPEED			7970E SPEED			EX. PART NUMBER 07970-	REPLACEMENT PART NO. 07970-	COMMENTS
		10-20.9	21-37.5	10-25	25.1-37.5	10-20.9	21-45	ALL	10-20.9	21-45	ALL	10-20.9	21-45	ALL			
7580	Head Assy R/W 9tr 21-45 IPS		X				X								N/A	62206	
581	Head Assy R/W 7tr 21-45 IPS		X				X								N/A	62204	
582	Head Assy RO 9tr 21-45 IPS		X				X								N/A	62202	
583	Head Assy RO 7tr 21-45 IPS		X				X								N/A	62200	
584	Head Assy R/W 7tr 10-20.9 IPS	X				X									N/A	62203	
585	Head Assy R/W 9tr 10-20.9 IPS	X				X									N/A	62211	
586	Head Assy R/O 7tr 10-20.9 IPS	X				X									N/A	62199	
587	Head Assy R/O 9tr 10-20.9 IPS	X				X									N/A	62201	
588	Head Assy R/R 7/9tr 10-20.9 IPS	X				X									N/A	62207	
589	Head Assy R/R 7/9tr 21-45 IPS		X				X								N/A	62208	
600	Dual Chan. Write	X				X									N/A		
610	Dual Chan. Write		X				X								N/A		
620	Single Chan. Write	X				X									N/A		
630	Single Chan. Write		X				X								N/A		
650	Read Parity 9tr	X	X					X							N/A	60954	
651	Write Parity 9tr	X	X					X							N/A		
652	Write Parity 7tr	X	X					X							N/A		
653	Read Parity 7tr	X	X					X							N/A		
654	Prog. Read Parity 7/9tr	X	X					X						X	69333		Note 5.
810	Power Regulator				X			X						X	N/A		Note 4.
820	Power Distribution				X			X						X	N/A		Note 4.
830	Door Interlock	X	X					X						X	N/A		
860	Real Servo				X										61061	62173	
870	Capstan Servo				X										61071	62172	
880	Control & Status				X										61081	62336	

HP PART NUMBER 07970-	ASSEMBLY DESCRIPTION	7970A SPEED				7970B SPEED			7970C SPEED			7970E SPEED			EX. PART NUMBER 07970-	REPLACEMENT PART NO. 07970-	COMMENTS
		10-20.9	21-37.5	10-25	25.1-37.5	10-20.9	21-45	ALL	10-20.9	21-45	ALL	10-20.9	21-45	ALL			
62130	Aux. Control										X				69326		
62131	Photosense Assy.							X			X			X	N/A	62345	
62132	Power Supply										X				N/A		
62133	Control & Status										X				69327		
62134	Capstan Servo Assy.										X				69328		
62135	Control Switch Assy.										X				N/A		
62136	Aux. Control Switch										X				N/A		
62138	Power Regulator										X				69329		
62140	Reel Servo Assy.										X				69330		
62141	Power Distribution Assy.										X				N/A		
62143	Write Control										X				N/A		
62144	Single Chan. Write									X					N/A		
62145	Dual Chan. Write									X					N/A		
62147	Read Control									X					N/A		
62165	Write Interconnect	X				X									N/A		
62166	Dual Chan. Read	X				X						X			N/A		Note 5
62167	Single Chan. Read	X				X						X			N/A		Note 5
62168	Dual Chan. Read		X				X						X		N/A		Note 5
62169	Single Chan. Read		X				X						X		N/A		Note 5
62170	Read Control	X				X									N/A		
62171	Read Control		X				X								N/A		
62172	Capstan Servo				X			X						X	62245		
62173	Reel Servo				X			X						X	62244		
62177	Triple Density Select 7/9tr							X							N/A		
62199	H[illegible] Assy. R/O 7tr	X				X	[illegible]								N/A		[illegible]

PART NUMBER 970-	ASSEMBLY DESCRIPTION	7970A SPEED				7[illegible] SPEED			7970C SPEED			7970E SPEED			EX. PART NUMBER 07970-	REPLACEMENT PART NO. 07970-	COMMENTS
		10-20.9	21-37.5	10-25	25.1-37.5	10-20.9	21-45	ALL	10-20.9	21-45	ALL	10-20.9	21-45	ALL			
42	P.E. Read Control													X	62129	62278	
43	P.E. Data & Status													X	62127		
49	Dual Chan. Write 21-45 IPS												X		N/A		
50	Single Chan. Write 21-45												X		N/A		
51	P.E. Write Interconnect													X	N/A		
52	Dual Chan. Write 10-20.9 IPS											X			N/A		
53	Single Chan. Write 10-20.9 IPS											X			N/A		
70	Read Only Mother Bd NRZI													X	N/A		Note 5.
71	Read Control NRZI 21-45 IPS												X		N/A		Note 5.
72	Control & Status													X	62128		
71	P.C. Power Distribution													X	N/A		
72	Power Regulator													X	N/A		
74	R/R/R Pre Amp 10-20.9 IPS													X	N/A		Note 5.
86	Unit Select Assy.							X						X	N/A		
87	Triple Density Select							X							N/A		
88	R/R Density Select							X							N/A		
89	Control Switch Assy.							X						X	N/A		
92	Read Control NRZI 10-20.9					X									N/A		Note 5.
49	Density Select Multiformat													X	N/A		Note 5.
50	Dual Density Select													X	N/A		Note 5.
51	Parity Select													X	N/A		Note 5.
52	Control Switch Assy.							X						X	N/A	62089	
53	Tension Arm Assy.							X						X	N/A		
21	Head [illegible]sy. Dual Speed 7/9tr											X			N/A		
22	Write Enable Assy.																

PART NUMBER 7970-	ASSEMBLY DESCRIPTION	7970A SPEED				0B SPEED			7970C SPEED			7970E SPEED			EX. PART NUMBER 07970-	REPLACEMENT PART NO. 07970-	COMMENTS
		10-20.9	21-37.5	10-25	25.1-37.5	10-20.9	21-45	ALL	10-20.9	21-45	ALL	10-20.9	21-45	ALL			
2200	Head Assy. R/O 7tr		X				X								N/A		
2201	Head Assy. R/O 9tr	X				X									N/A		
2202	Head Assy. R/O 9tr		X				X								N/A		
2203	Head Assy. R/W 7tr	X				X									N/A		
2204	Head Assy. R/W 7tr		X				X								N/A		
2205	Head Assy. R/W 9tr	X				X									N/A		
2206	Head Assy. R/W 9tr		X				X			X					N/A		
2207	Head Assy. R/R 7/9tr	X				X									N/A		
2208	Head Assy. R/R 7/9tr		X				X								N/A		
2209	Head Assy. R/O											X			N/A		
2210	Head Assy. R/O												X		N/A		
2211	Head Assy. R/W 9tr					X									N/A		
2212	Head Assy. R/W 9tr												X		N/A		
2213	Head Assy. R/R 7/9tr											X			N/A		
2214	Head Assy. R/R 7/9tr												X		N/A		
2246	Head Assy R/O 9tr						X								N/A	62210	
2248	Head Assy. R/W 9tr					X									N/A		
2266	P.E. Read Control													X	62279		
2301	Head Assy. R/R 9tr												X		N/A		
2344	Decoder													X	N/A	62353	
2387	Read Pre Amp					X									62298		Note 2
2399	R/R Density Select							X							N/A		
2316	Single Chan. Read									X					N/A		
2317	Dual Chan. Read									X					N/A		
2324	48 VDC Supply							X			X			X	69324		

HP PART NUMBER 07970-	ASSEMBLY DESCRIPTION	7970A SPEED				7970B SPEED			7970C SPEED			7970E SPEED			EX. PART NUMBER 07970-	SUPPLEMENT PART NO. 07970-	COMMENTS
		10-20.9	21-37.5	10-25	25.1-37.5	10-20.9	21-45	ALL	10-20.9	21-45	ALL	10-20.9	21-45	ALL			
62325	Read Pre Amp									X					69325		
62335	P.C. Card Cage													X	N/A		
62336	Control & Status							X							69331		
62345	Photosense Assy.							X			X			X	N/A		
62348	Write Enable Assy.							X						X	N/A		Note 6
62363	Decoder													X	N/A		
62363	60 VDC Supply							X						X	N/A		
62364	60 VDC Assy.							X						X	69364		
62369	HP-IB Control													X	N/A		
62370	HP-IB Write Formatter													X	N/A		
62381	HP-IB Assy.													X	69381		

NOTE 1: Serial prefix 1208 and below.

NOTE 2: Used only with 07970-62031 head.

NOTE 3: Used only with the following heads:

07970-60584
*07970-60585
07970-60586
07970-60587

NOTE 4: Used in P.E. Slave.

NOTE 5: Multiformat 7970E only.

NOTE 6: Use only on 7970's with either 48 or 60 VDC supply.

* Now obsoleted. Returned head will be automatically replaced by 07970-62205 head.

7970B/C-3-76
7970E-4-76

P R O D U C T I O N M E M O

TO: "MAILS"

FROM: BOISE DIVISION PRODUCT SUPPORT

SUBJECT: HEAD GATE ASSEMBLY REPLACEMENT ON 7970 READ AFTER WRITE HEADS

The head gate assemblies, (see figure 1) on most of the early 7970 heads can be replaced if the existing head gate is damaged. This will eliminate the need to send the entire assembly to Mt. View for repair of the head gate.

The head assemblies that may be field repaired are:

HP P/N	DESCRIPTION	TAPE DRIVE MODEL
07970-60580	9 Tr NRZI 21-45 IPS	7970A, 7970B & 7970C
07970-60581	7 Tr NRZI 21-45 IPS	7970A, & 7970B
07970-60584	7 Tr NRZI 10-20.9 IPS	7970A, & 7970B
07970-60585	9 Tr NRZI 10-20.9 IPS	7970A, & 7970B
07970-62028	9 Tr P.E. 21-45 IPS	7970E
07970-62031	9 Tr P.E. 10-20.9 IPS	7970E

Replacement Part Ordering.

Compare the face of the head gate assemblies shown in figures 2 thru 6 to the assembly on 7970 head under repair,to find the correct part number. Do not change the style of head gate.

INSTALLATION

1. Remove the 7970 head assembly from the tape drive.
2. Remove the head gate assembly from the head assembly.
   NOTE: Use extreme caution when removing the headgate to prevent scratching the face of the head. Any hard part or tool may cause severe damage. Tape a small piece of punch card across the face of the Read/Write head to prevent scratching the head and provide a distance gage for headgate clearance.
3. Install the new head gate assembly.
4. Re-install the head assembly in the tape drive.
5. Load a scratch tape on the tape drive.
6. Install both the 13191A Control & Status test PCA and 13192A Write Test PCA. Place all switches on the 13191A in the down position.

BG/11/WN

2/76-46

HEWLETT hp PACKARD

7. Place the switches on the 13192 in the following position:

xtalk/Block	-	xtalk position
odd/even	-	odd position
7tr/9tr	-	in 7tr or 9tr depending upon tape drive.

8. Apply power and place the tape drive ON-LINE.

9. Place the WSW and CF switches on the 13191A Control Status Test PCA in the up position, until the WS LED on the 13192A Write Test PCA comes on. Place the CF switch on the 13191A in the down position to stop tape. NOTE: The WS LED on the 13192A should remain on.

10. Connect an oscilloscope to the WCD test point on the Write Control PCA and adjust the potentiometer on the 13192A PCA for the appropriate bit to bit time to write 200 BPI. The formula is as follows:

$$\frac{1}{\text{Density x Speed}} = \text{Clock Rate}$$

Example

$$\frac{1}{200 \times 25} = \frac{1}{5000} = 200\text{usec Bit to Bit for 25 IPS machine}$$

11. Move the oscilloscope probe to test point P on the preamp PCA and place the CF switch on the 13191A in the up position (tape should move forward). Adjust the voltage to 6.4 volts peak to peak. Check and adjust the remainder of the preamp test points to the same amplitude.

12. Stop tape motion by placing the CF switch in the down position.

    NOTE: Write head current remains on when the CF switch is in the off position. Write current will be turned off under the following conditions:

    1. Tape drive is issued a motion command other than CF.
    2. WSW command is turned off and a CF command is given. In this situation, just turn off CF because in order to check the crosstalk in step 13 current must be flowing in the write heads.

13. With the oscilloscope, check the signal amplitude on the preamp test points and ensure it does not exceed 5% of the peak to peak amplitude set in step 11 (or 320 millivolts). If the amplitude exceeds the specification, remove the Read/Write head assembly and adjust the head gate closer to the face of the head. NOTE: DO NOT allow the head gate to come nearer than two (2) thicknesses of mylar tape.

    Install the head assembly and repeat steps 11 thru 13.

14. Verify the complete alignment of data electronics

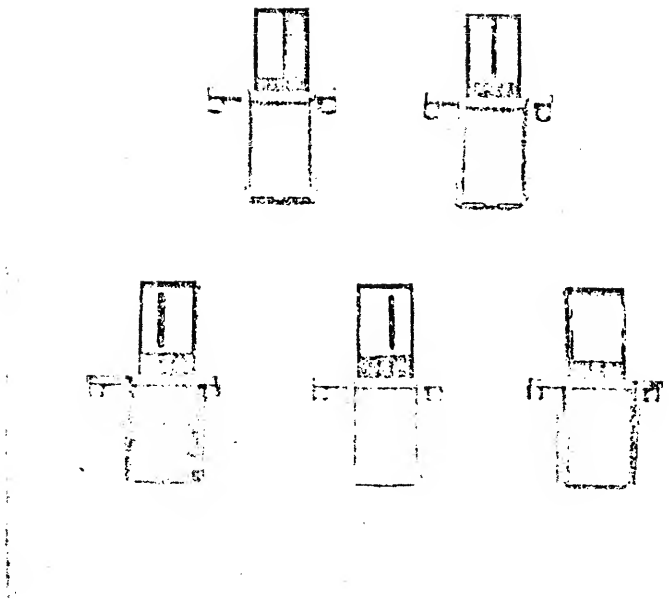


Figure 1 Headgate assemblies

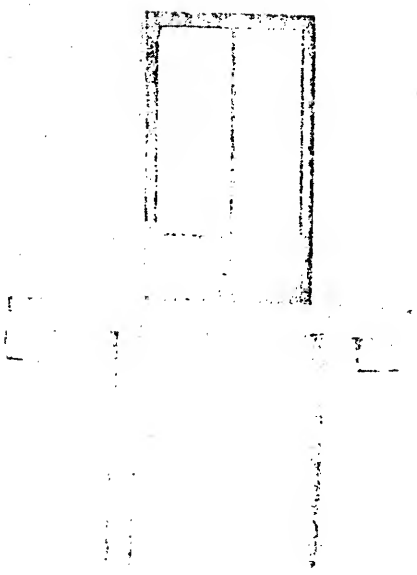


Figure 2
07970-62338

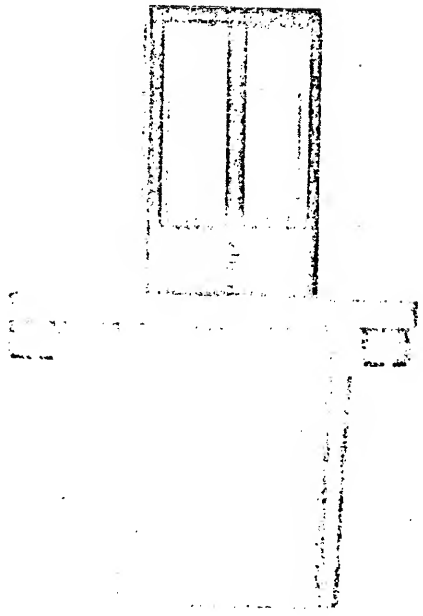


Figure 3
07970-62339

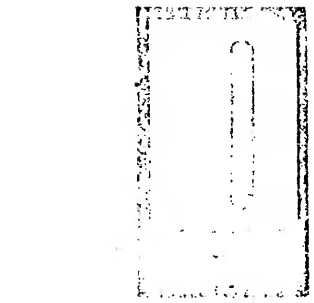


Figure 4
07970-62340

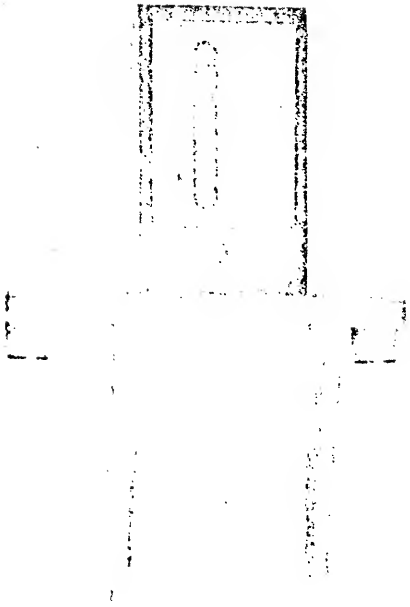


Figure 5
07970-62341

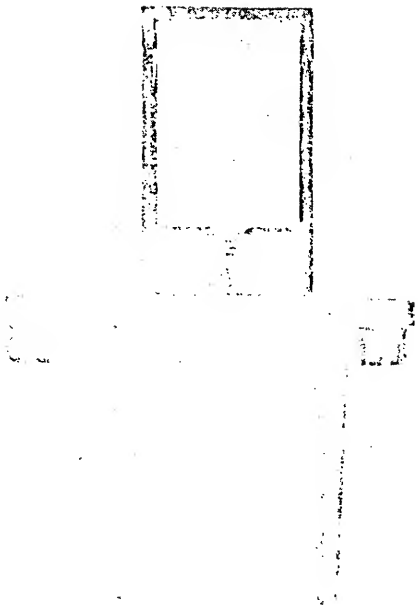


Figure 6
07970-62342